

SA9137 USB Audio Streaming Controller

1. Features

- Supply Range of 1.8 V to 3.3 V
- Control and I/O
 - I2C bus Master
 - FWIOs
- Support iAP2
- USB 2.0 High-Speed Compliant
- USB Audio Class v1.0 and v2.0 supported
- Support Dynamic Consumption Adjustment
- One interrupt endpoint for HID
- Support DSD64 / DSD128 / DSD256 both of native and DoP in Async mode
- Support DSD L/R data line swap feature
- Support resolutions up to 32-bit and sampling rates up to 384KHz
- Support 2ch playback
- Support 2ch record
- Support fixed DMCLK mode
 - 11.2896/ 12 / 12.288 / 22.5792/ 24.576MHz
- One I2S input and one I2S output pairs for PCM
 - Independent sample rates for each pair
 - 32/ 44.1/ 48/ 88.2/ 96/ 176.4/ 192/ 352.8/ 384 KHz sampling rates
 - 16/24/32-bit resolution
- 48-pin QFN package

2. Description

- Mobile Phone Audio Accessary
- Type-C Audio
- USB Audio

3. Applications

The SA9137 is a high-performance up to 32bit, 384KHz PCM and DSD64/128/256 streaming USB High-Speed compliant audio steaming controller. It features one IEC60958 S/PDIF transmit streaming output. The SA9137 is ideal for both one stereo-in and one stereo-out professional digital audio interface applications. Its PCM resolution and sampling rate can be configurable with 16/24/32

Device Information

PART NUMBER	PACKAGE	BODY SIZE
SA9137	QFN-48	6mm x 6mm

4. Simplified Schematic

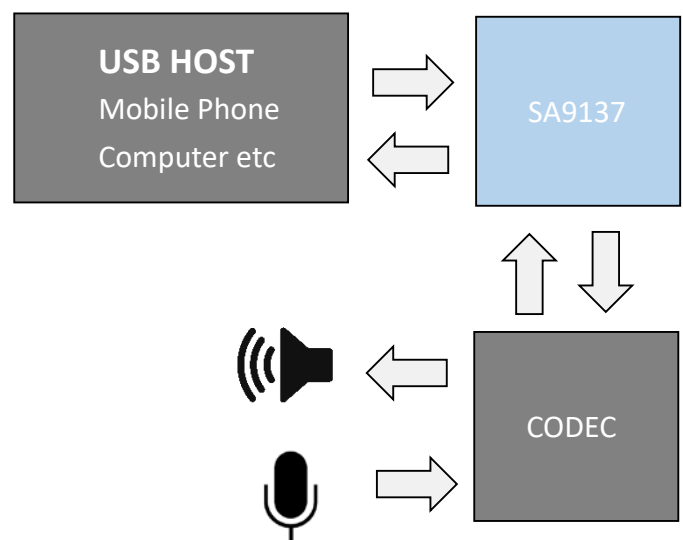


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5. Pin Configuration and Functions

5.1 Pin Configuration

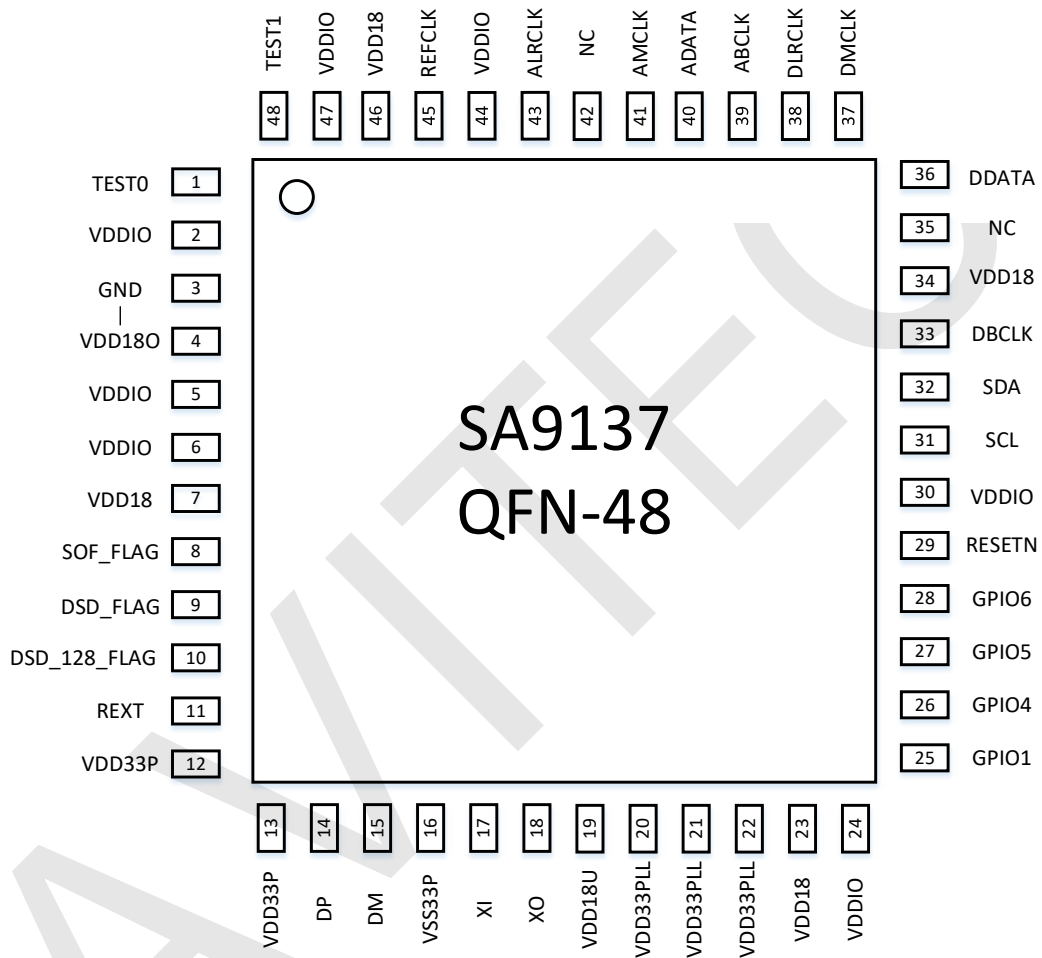


Figure 5-1. QFN-48 Pin Diagram (Top View)

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5.2 Pin Functions

PIN		TYPE	DESCRIPTION
NAME	TQFP-80		
TEST0	1	Ground	normal mode: connect to GND
VDDIO	2	Power	VDDIO 1.8V to 3.3V
GND	3	Ground	GND
VDD18O	4	Power	Connect 1uF to Ground
VDDIO	5	Power	VDDIO 1.8V to 3.3V
VDDIO	6	Power	VDDIO 1.8V to 3.3V
VDD18	7	Power	1.8V Core power
SOF_FLAG	8	O	USB Start-Of-Frame indicator
DSD_FLAG	9	O	DSD/PCM indicator
DSD_128_FLAG	10	O	DSD64/DSD128 indicator
REXT	11	I	Connect to 270ohm resistor to ground
VDD33P	12	Power	USB2.0 PHY 3.3V power
VDD33P	13	Power	USB2.0 PHY 3.3V power
DP	14	I/O	USB2.0 signals
DM	15	I/O	USB2.0 signals
VSS33P	16	Ground	Ground
XI	17	I	12MHz X'stal input
XO	18	O	12MHz X'stal output
VDD18U	19	Power	USB2.0 PHY 1.8V power
VDD33PLL	20	Power	3.3V PLL Power
VDD33PLL	21	Power	3.3V PLL Power
VDD33PLL	22	Power	3.3V PLL Power
VDD18	23	Power	1.8V Core power
VDDIO	24	Power	VDDIO 1.8V to 3.3V
GPIO1	25	I/O	Firmware assign function I/O port ^{*1}
GPIO4	26	I/O	Firmware assign function I/O port ^{*1}
GPIO5	27	I/O	Firmware assign function I/O port ^{*1}
GPIO6	28	I/O	Firmware assign function I/O port ^{*1}
RESETN	29	I	Power-on reset signal (Active low)
VDDIO	30	Power	VDDIO 1.8V to 3.3V

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SCL	31	O	Master I2C clock
SDA	32	I/O	Master I2C data
DBCLK	33	I/O	I2S Playback BCLK
VDD18	34	Power	1.8V Core power
NC	35	-	floating
DDATA	36	O	I2S Playback DATA
DMCLK	37	I/O	I2S Playback MCLK
DLRCLK	38	I/O	I2S Playback LRCLK
ABCLK	39	I/O	I2S Record BCLK
ADATA	40	I	I2S Record DATA
AMCLK	41	I/O	I2S Record MCLK
NC	42	-	floating
ALRCLK	43	I/O	I2S Record LRCLK
VDDIO	44	Power	VDDIO 1.8V to 3.3V
REFCLKIN	45	I	External reference clock input
VDD18	46	Power	1.8V Core power
VDDIO	47	Power	VDDIO 1.8V to 3.3V
TEST1	48	Ground	normal mode: connect to GND

*1. All FWIOs are firmware assign function input/output, contact FAE to customize.

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6. Specifications

6.1 DC Characteristics

Test Conditions: Ta = 25°C; VDD33 = +3.0 ~ +3.6V; fs = 48 kHz-32bit sine wave

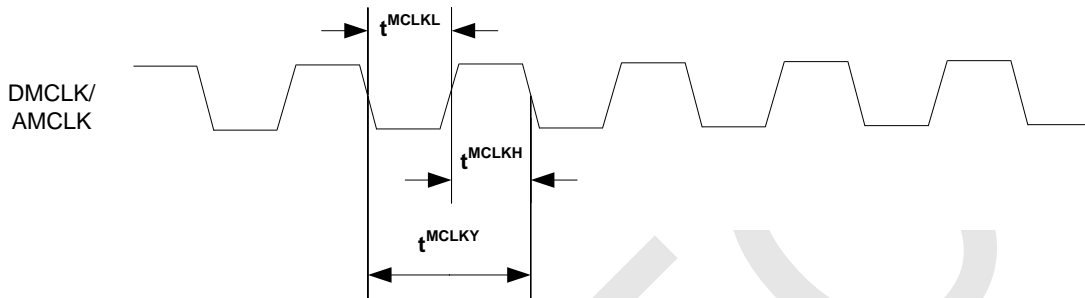
			MIN	TYP	MAX	UNIT
Input Low Voltage	VIL	VDD33 = 3.3V		0.3*VDD33		V
Input High Voltage	VIH	VDD33 = 3.3V	0.7*VDD33			V
Output Low Voltage	VOL	IOL = 2mA		0.2		V
Output High Voltage	VOH	IOH = 2mA	VDD33-0.2			V
Input Low Leakage Current	IIL	VIN = 0V VDD33 = 3.6V		10		uA
Input High Leakage Current	IIH	VIN = 3.6V VDD33 = 3.6V		10		uA
Operation Current	Idle ^{*1}	VDD33 = 3.3V VDD18 = Ext. DC-DC		30		mA
Operation Current	Up to 192KHz Playback ^{*1}	VDD33 = 3.3V VDD18 = Ext. DC-DC		45		mA
Operation Current	Up to 384KHz & DSD Playback ^{*2}	VDD33 = 3.3V VDD18 = Ext. DC-DC		66		mA
Suspend Current	Suspend	Total 3.3V rail	2	3		mA
		Total 1.8V rail	2	3		

*1 The power mode is controlled by F/W. This mode can not support DSD.

*2 Support DSD up to DSD128 by DoP and DSD256 by native DSD.

6.2 AC Timing Characteristics

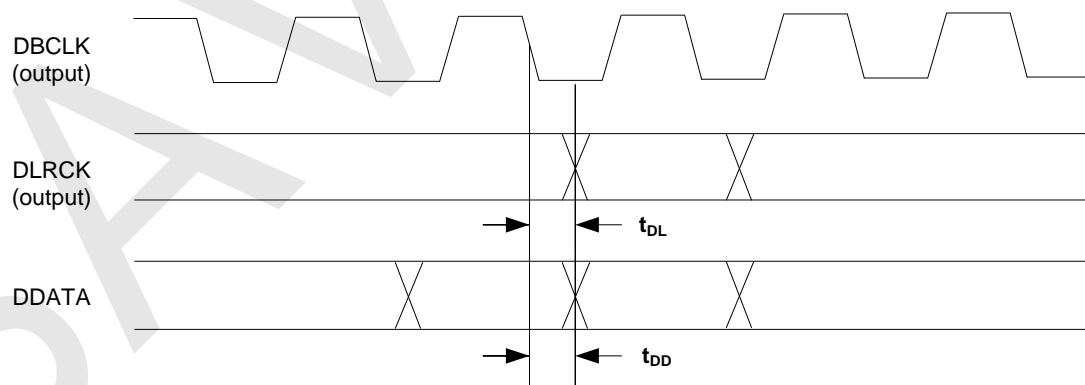
6.2.1 System Clocking Timing



Test Conditions: VDD = 3.3V, VSS = 0V, TA = +25°C, Master Mode fs = 48kHz, MCLK = 256fs, 24--bit data.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
DMCLK/AMCLK System clock pulse width high	t_{MCLKL}		41.13		ns
DMCLK/AMCLK System clock pulse width low	t_{MCLKH}		40.23		ns
DMCLK/AMCLK System clock cycle time	t_{MCLKY}		81.36		ns

6.2.2 Audio Interface Timing – Master Mode



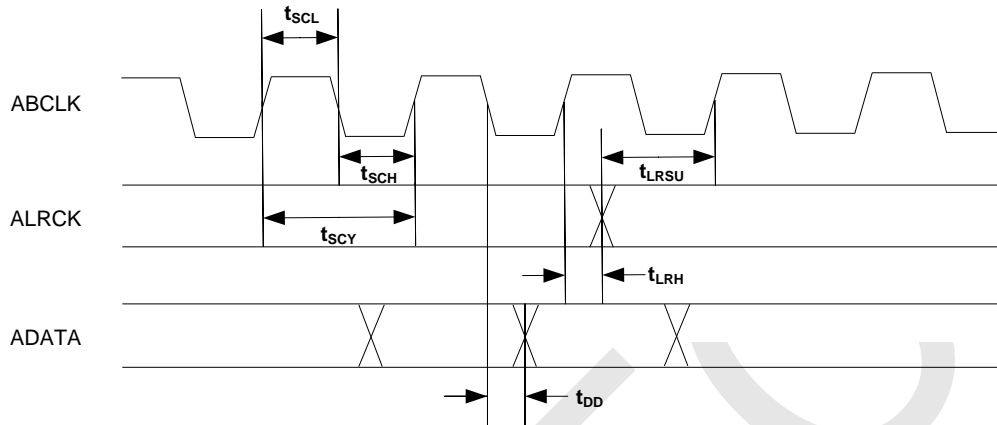
Test Conditions: VDD = 3.3V, VSS = 0V, TA = +25°C, Master Mode fs = 48kHz, MCLK = 256fs, 24--bit data.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
DLRCK propagation delay from DBCLK falling edge	t_{DL}	5			ns
DDATA propagation delay from DBCLK falling edge	t_{DD}	5			ns

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6.2.3 Audio Interface Timing – Slave Mode



Test Conditions: VDD = 3.3V, VSS = 0V, TA = +25°C, Master Mode fs = 48kHz, MCLK = 256fs, 24--bit data.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
ABCLK cycle time	t_{SCY}	293	325	358	ns
ALRCK pulse width high	t_{SCH}	144	163	178	ns
ABCLK pulse width low	t_{SCL}	144	163	179	ns
ALRCK set-up time to ABCLK rising edge	t_{LRSU}	10			
ALRCK hold time from ABCLK rising edge	t_{LRH}	10			
ADATA propagation delay from ABCLK falling edge	t_{DD}	5			

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6.3 Dynamic Electrical Characteristics (DP/DM)

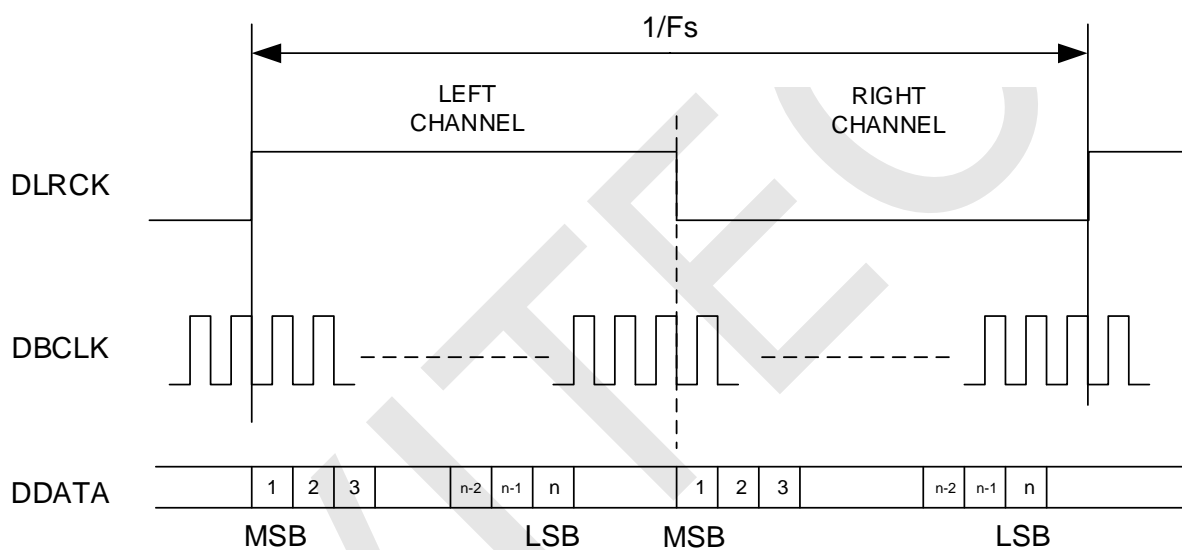
Driver Characteristics:

PARAMETER	SYMBOL	MIN	MAX	UNIT
High – Speed Mode				
High – speed differential rise time (10% - 90%)	t_{HSR}	500		ps
High – speed differential fall time (10% - 90%)	t_{HSF}	500		ps
Full – Speed Mode				
Rise Time for DP/DM	t_{FR}	4	20	ns
Fall Time for DP/DM	t_{FF}	4	20	ns
Differential Rise/Fall Time Matching (t_{FR}/t_{FF})	t_{FRFM}	90	110	%
Output Signal Crossover Voltage	V_{CRS}	1.3	2.0	V

7. Serial Audio Interfaces Formats

7.1 L - Justified Format

In Left Justified mode, the MSB is available on the first rising edge of DBCLK following an DLRCK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, DBCLK frequency and sample rate, there may be unused DBCLK cycles before each DLRCK transition.

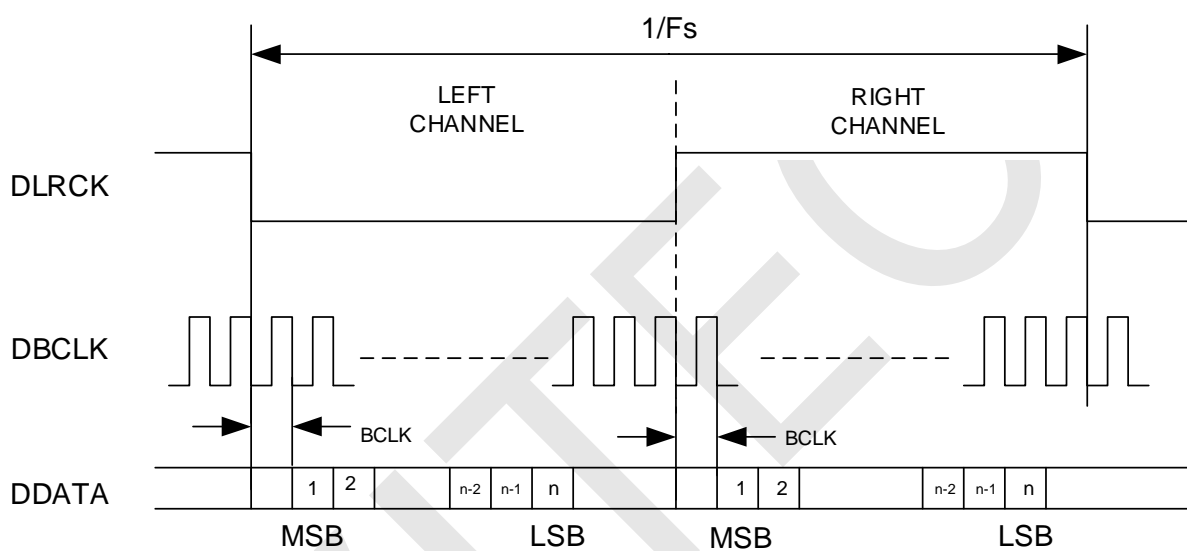


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7.2 I2S Format

In I2S mode, the MSB is available on the second rising edge of DBCLK following an DLRCK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, DBCLK frequency and sample rate, there may be unused DBCLK cycles between the LSB of one sample and the MSB of the next.



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7.3 Fixed DMCLK Mode

SA9137 supports four different MCLKs during fix mode^{*1} which can generate high precision clock for DAC/CODEC/ADC.

- 11.2896Mhz
- 12Mhz
- 12.288Mhz
- 22.5792Mhz
- 24.576Mhz

^{*1} The fix mode is controlled by F/W.

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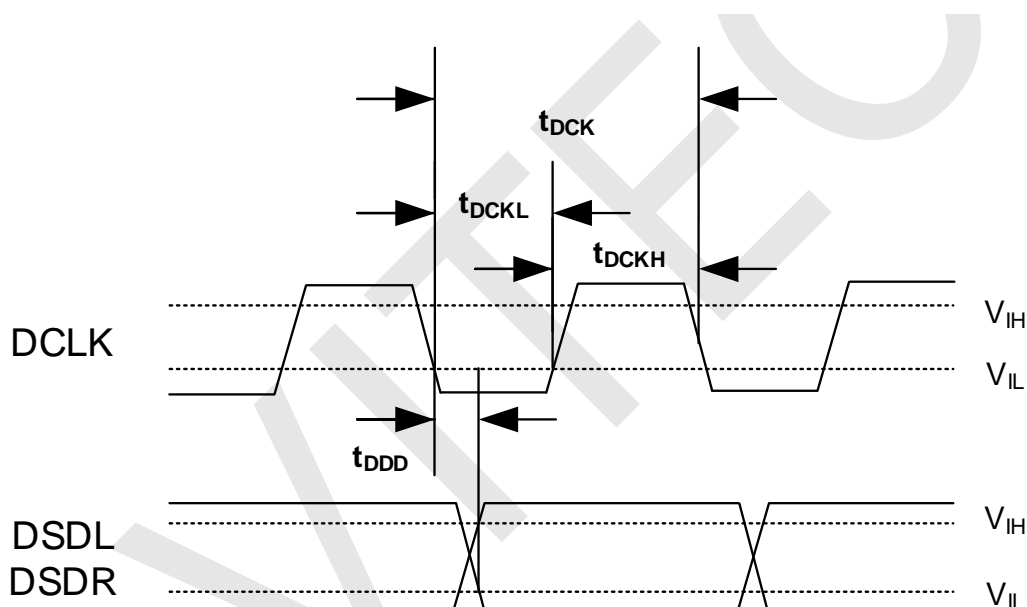
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8. DSD Audio Data Interfaces

SA9137 supports five modes for playback DSD data over USB Audio streaming

PARAMETER	DCLK	DSD Mode
DSD 64 for 88.2K 32-bit	DCLK(2.8224MHz)	Direct DSD
DSD 128 for 176.4K 32-bit	DCLK(5.6448MHz)	Direct DSD
DSD 256 for 352.8K 32-bit	DCLK(11.2896MHz)	Direct DSD
DSD 64 for 176.4K 24-bit	DCLK(5.6448MHz)	DoP/dCS
DSD 128 for 352.8K 24-bit	DCLK(11.2896MHz)	DoP/dCS



The DSDL and DSDR are all output by negative edge of DCLK. And DSD DAC will sample them by post edge of DCLK.

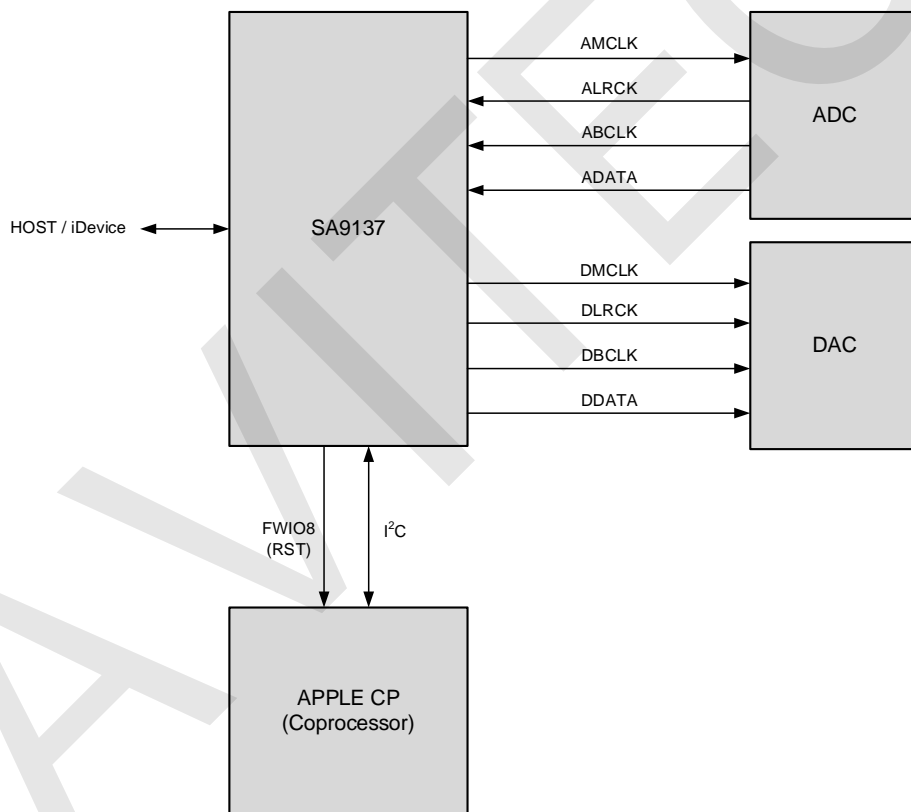
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9. iDevice Support

Apple strongly recommends the use of digital audio paths to and from accessories. Apple device in USB Host Mode audio is the recommended approach. SA9137 will authenticate and identify itself to Apple device using iAP2 CP before the iDevice will enumerate and start using USB Audio interface.

- Support 16 /24-bit linear PCM
- Support 44.1 / 48KHz sampling rate and up to 384KHz for future.
- Support input and output audio interface
- Support Volume Control Feature Unit
- Support iAP2 by CP2.0B and CP2.0C.



Digital USB Audio Application For iDevice

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10. S/PDIF TX Interface

SA9137 support one S/PDIF TX interface, each can support up to 24-bit 384K sampling rate. Built in IEC60958 professional S/PDIF TX.

- AES/EBU supported
- DSD stream output on S/PDIF TX
- 32/ 44.1/ 48/ 88.2/ 96/ 176.4/ 192/ 325.8/ 384KHz sampling rates
- 16/24 bit resolution

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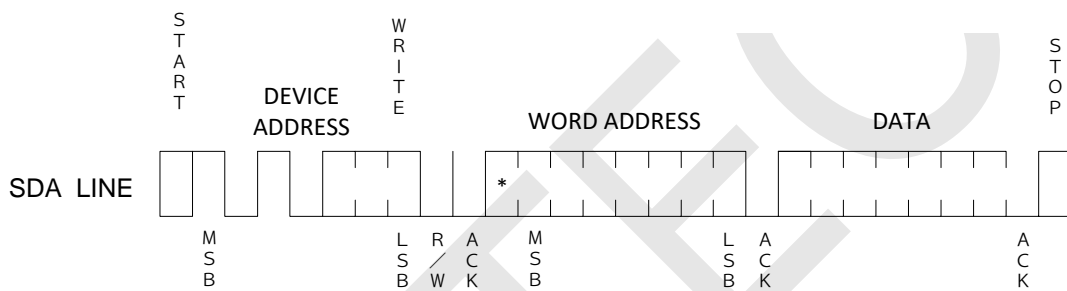
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11. I²C Master Interfaces

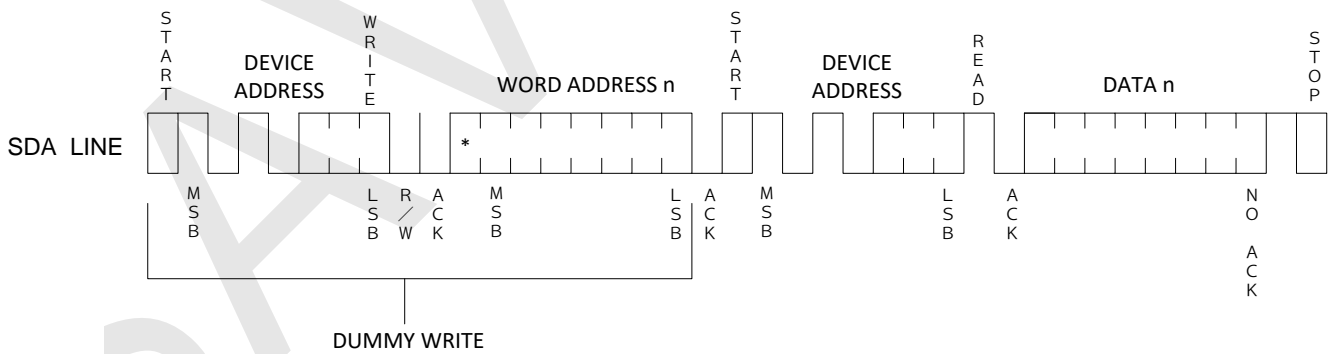
One serial I²C master is supported in SA9137 to control external peripheral devices (EEPROM). SA9137 need an EEPROM to load Firmware code from it.

SA9137 support use I²C Master Interfaces to read/write CP to support Apple MFi.

Byte Write



Random Read



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12. Chip Status Flags

SA9137 provide these pins for display chip status flag

FLAG	Definition
DSD_FLAG	User can check this pin to understand DSD mode is detected or not 0: PCM mode 1: DSD mode
DSD_128_FLAG	User can check this pin to understand which DSD mode is played now (DSD64 or DSD128 mode) 0: DSD 64 mode 1: DSD 128 mode
SOF_FLAG	USB Start-Of-Frame indicator

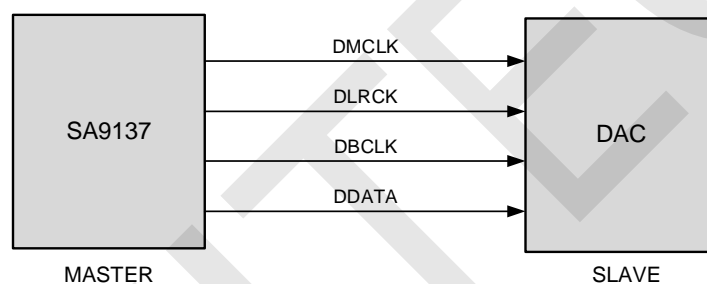
13. Application and Implementation

13.1 Typical Application

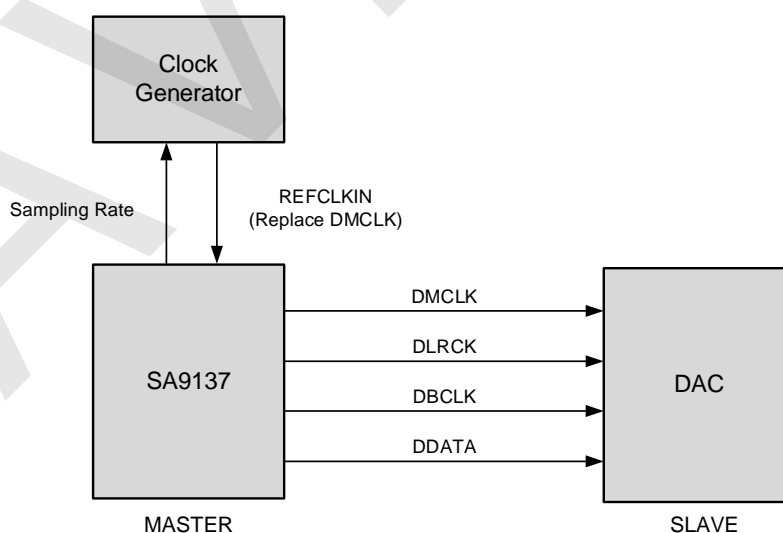
Typical application for SA9137 connecting with DAC / ADC. The following section shows how the SA9137 works with different serial data format including PCM & DSD.

13.1.1 Serial Audio Interfaces Configuration-DAC (Master Mode)

SA9137 supports master mode for following configuration



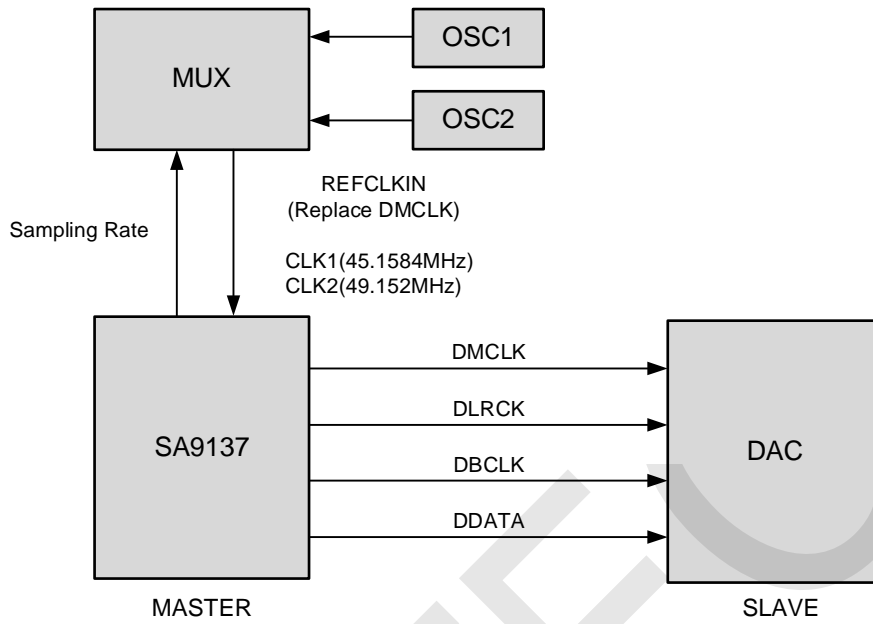
SA9137 I²S Mater Mode Connection



Master Mode (with external REFCLKIN), Mode 0

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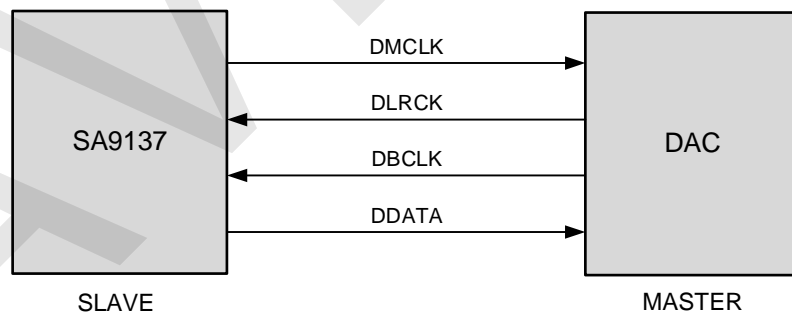
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Master Mode (with external REFCLKIN), Mode 1

13.1.2 Serial Audio Interfaces Configuration-DAC (Slave Mode)

SA9137 supports slave mode for following configuration



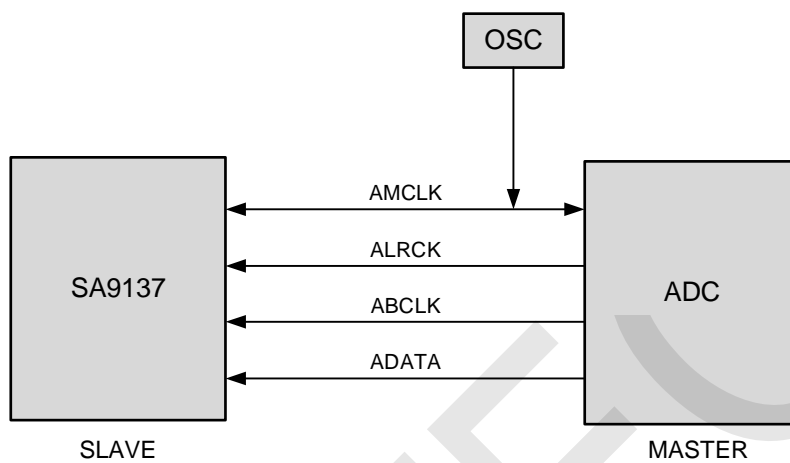
SA9137 I²S Slave Mode Connection

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13.1.3 Serial Audio Interfaces Configuration-ADC

SA9137 supports slave mode for following configuration



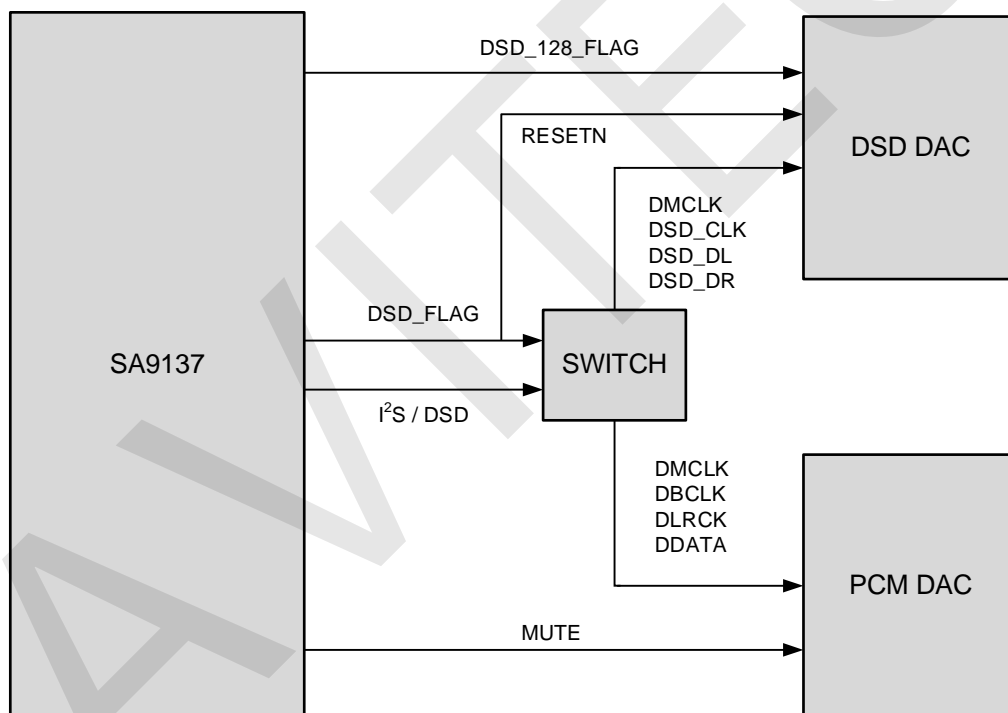
SA9137 I²S Slave Mode Connection

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13.1.4 DSD External Control Signals

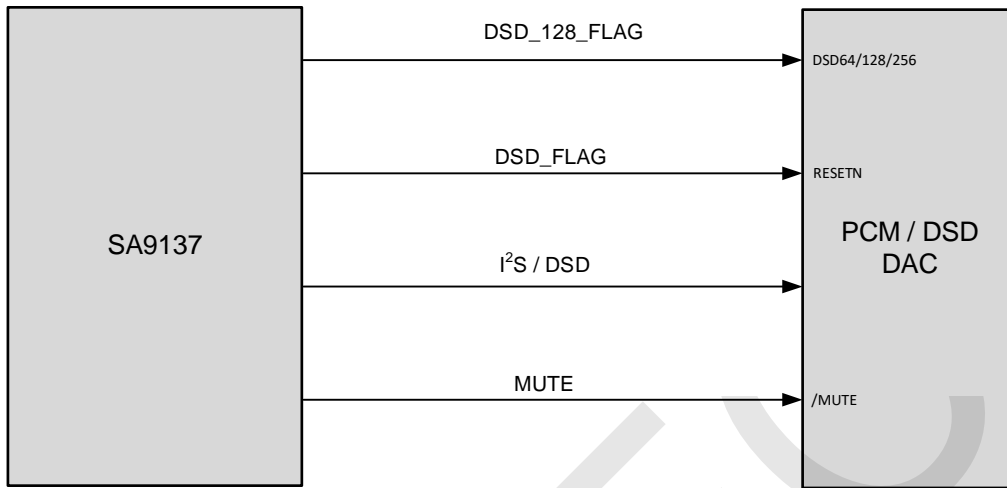
- DSD_FLAG : (0 : RESET, 1: Normal Operation in DSD format):
Used to RESETN DSD DAC.
- DSD_FLAG : (0 : in PCM mode, 1: in DSD mode):
Used to witch DSD or PCM DAC.
- DSD_128 : (0 : in DSD 64 mode, 1: in DSD 128 mode):
Used to switch DSD64 and DSD128 format for DSD DAC



Application with PCM DAC And DSD DAC

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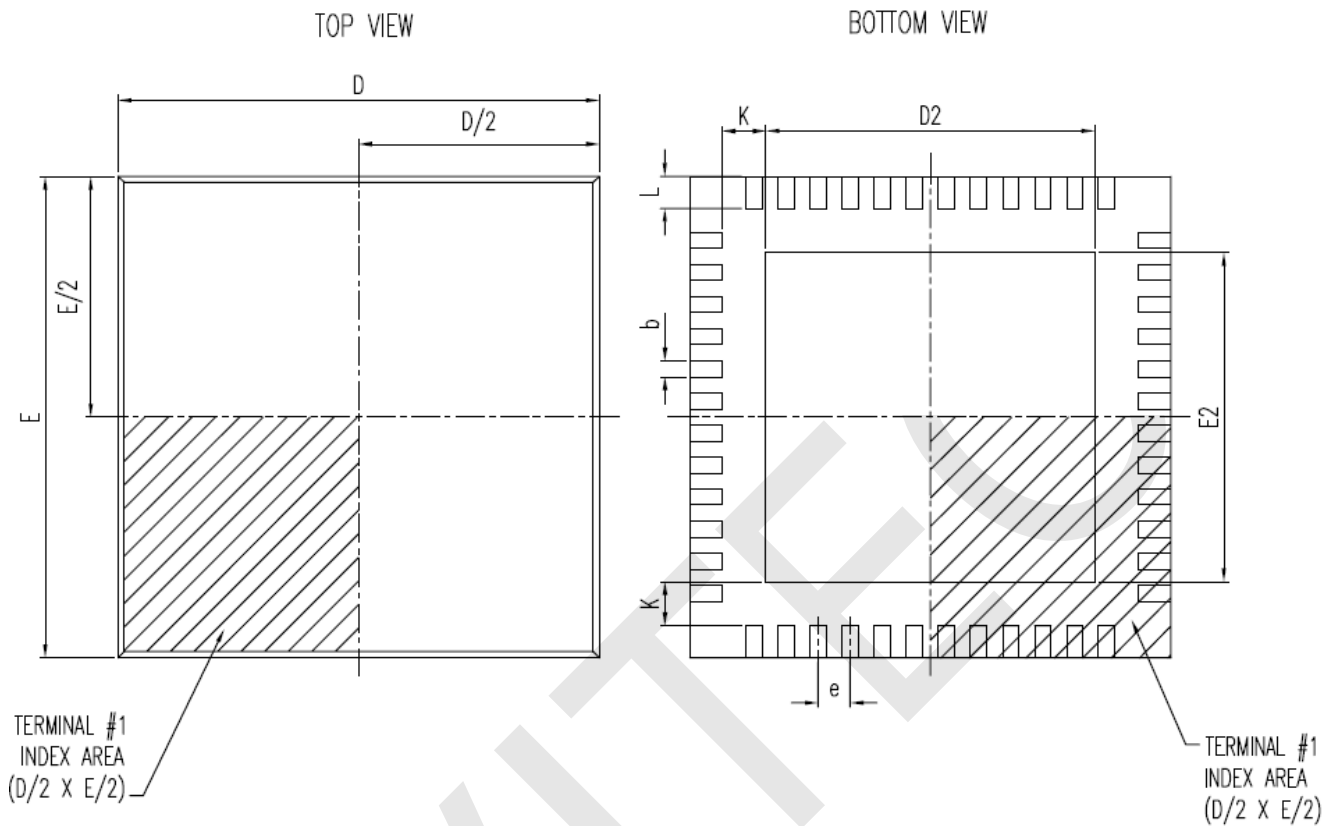


Application with PCM/DSD Multi Function DAC

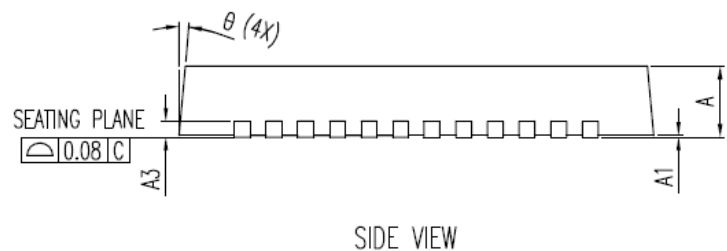
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14. Package Outline (QFN-48)


SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.20 REF.		
D	6.00 BASIC		
D2	3.95	4.10	4.25
E	6.00 BASIC		
E2	3.95	4.10	4.25
e	0.40 BASIC		
b	0.15	0.20	0.25
L	0.30	0.40	0.50
K	0.20		
θ	0°		14°
JEDEC	MO-220 (Variation WJJE)		



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15. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents

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