ES8218

Low Power Audio ADC

FEATURES

System

- High performance and low power multi-bit delta-sigma audio ADC
- I^2S/PCM master or slave serial data port
- Two pairs of analog input with differential input option
- 256/384Fs and USB 12/24 MHz system clocks
- Fast power up time
- I^2C interface

ADC

- 24-bit, 8 to 96 kHz sampling frequency
- 96 dB signal to noise ratio, -85 dB THD+N
- Low noise pre-amplifier
- Auto level control (ALC) and noise gate
- High PSRR
- Shelving filter to compensate mic frequency response
- Support digital mic

Low Power

- 1.8V to 3.3V operation
- 9 mW record
- Low standby current

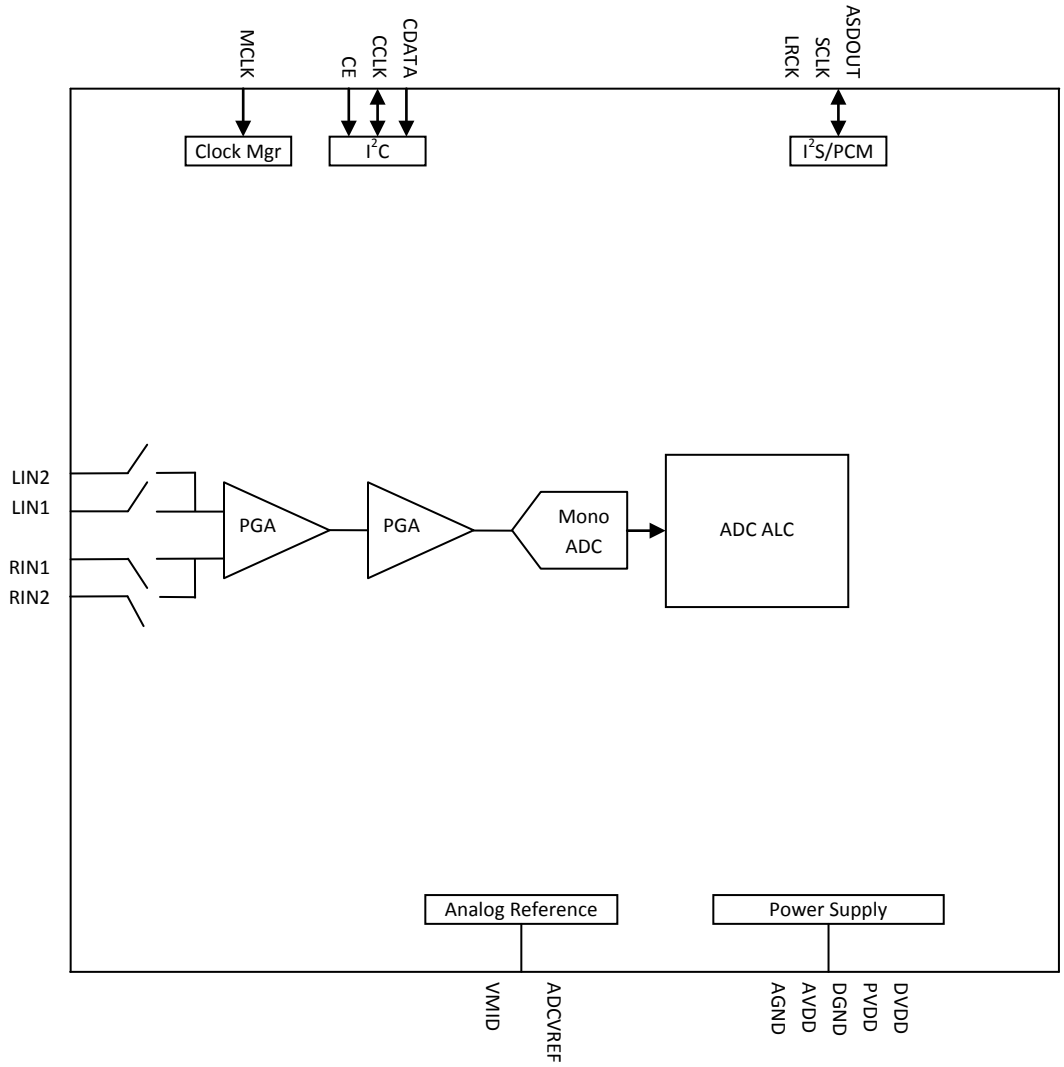
APPLICATIONS

- Wireless remote
- Portable audio

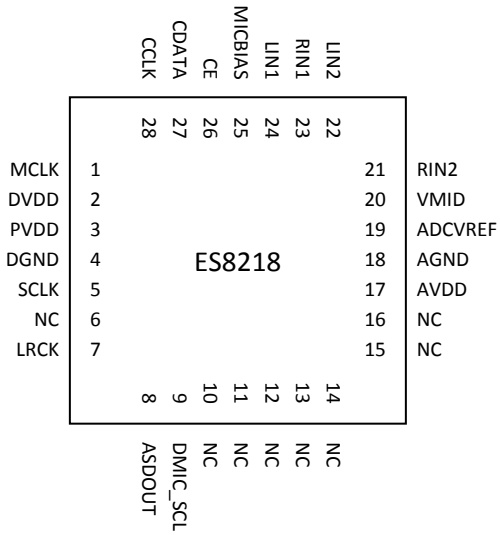
ORDERING INFORMATION

ES8218 -40°C ~ +85°C
QFN-28

1. BLOCK DIAGRAM

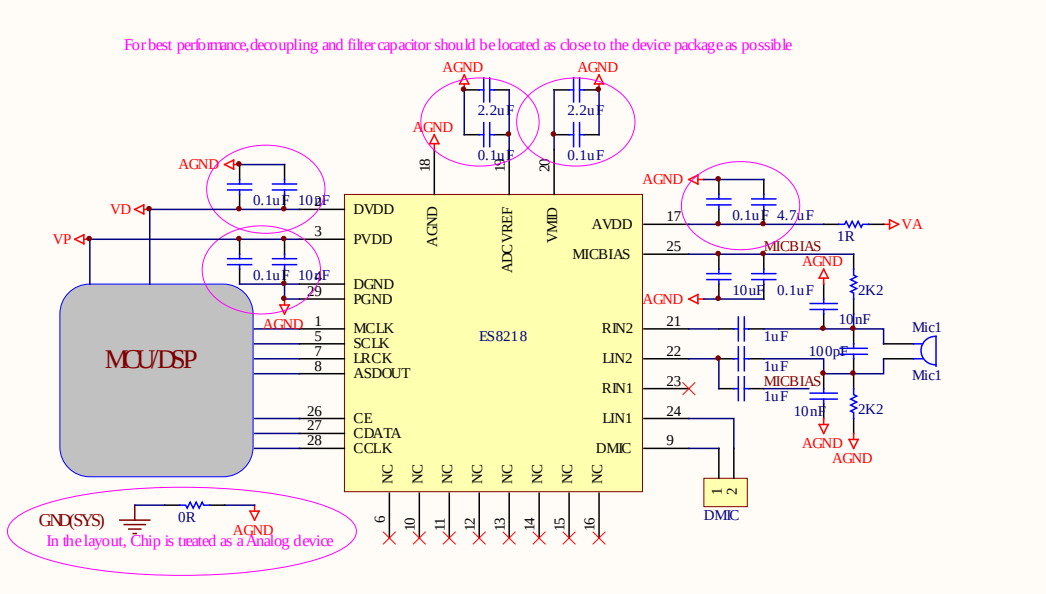


2. PIN OUT AND DESCRIPTION



PIN	NAME	I/O	DESCRIPTION
1	MCLK	I	Master clock
2	DVDD	Supply	Digital core supply
3	PVDD	Supply	Digital IO supply
4	DGND	Supply	Digital ground
5	SCLK	I/O	Audio data bit clock
6	NC		No connect
7	LRCK	I/O	Audio data left and right clock
8	ASDOUT	O	ADC audio data
9	DMIC_SCL		Digital mic clock
10	NC		No connect
11	NC		No connect
12	NC		No connect
13	NC		No connect
14	NC		No connect
15	NC		No connect
16	NC		No connect
17	AVDD	Supply	Analog supply
18	AGND	Supply	Analog ground
19	ADCVREF	O	Decoupling capacitor
20	VMID	O	Decoupling capacitor
21	RIN2	I	Right analog input
22	LIN2	I	Left analog input
23	RIN1	I	Right analog input
24	LIN1	I	Left analog input
25	MICBIAS		Mic bias
26	CE	I	I^2C device address selection
27	CDATA	I/O	I^2C data input or output
28	CCLK	I	I^2C clock input

3. TYPICAL APPLICATION CIRCUIT



4. CLOCK MODES AND SAMPLING FREQUENCIES

The device supports two types of clocking: standard audio clocks (256Fs, 384Fs, 512Fs, etc), and USB clocks (12/24 MHz).

According to the serial audio data sampling frequency (Fs), the device can work in two speed modes: single speed mode or double speed mode. In single speed mode, Fs normally ranges from 8 kHz to 48 kHz, and in double speed mode, Fs normally range from 64 kHz to 96 kHz.

The device can work either in master clock mode or slave clock mode. In slave mode, LRCK and SCLK are supplied externally, and LRCK and SCLK must be synchronously derived from the system clock with specific rates. In master mode, LRCK and SCLK are derived internally from device master clock.

5. MICRO-CONTROLLER CONFIGURATION INTERFACE

The device supports standard I^2C micro-controller configuration interface. External micro-controller can completely configure the device through writing to internal configuration registers.

I^2C interface is a bi-directional serial bus that uses a serial data line (SDA) and a serial clock line (SCL) for data transfer. The timing diagram for data transfer of this interface is given in Figure 1. Data are transmitted synchronously to SCL clock on the SDA line on a byte-by-byte basis. Each bit in a byte is sampled during SCL high with MSB bit being transmitted firstly. Each transferred byte is followed by an acknowledge bit from receiver to pull the SDA low. The transfer rate of this interface can be up to 400 kbps.

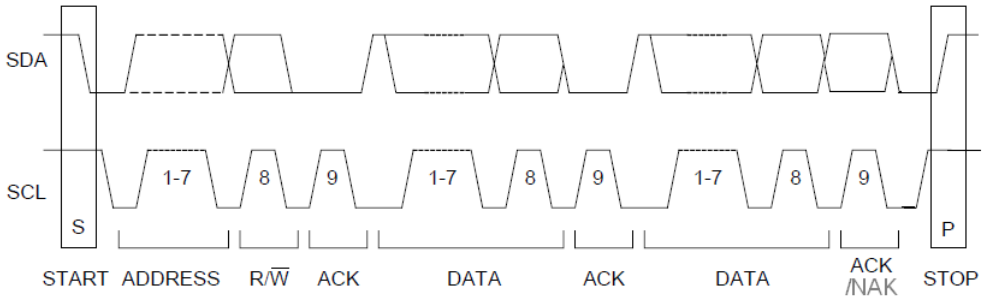


Figure 1 Data Transfer for I^2C Interface

A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at SDA while SCL is high. The first byte transferred is the slave address. It is a seven-bit chip address followed by a RW bit. The chip address must be 001000x, where x equals AD0. The RW bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the RW bit. The master can terminate the communication by generating a “stop” signal, which is defined as a low-to-high transition at SDA while SCL is high.

In I²C interface mode, the registers can be written and read. The formats of "write" and "read" instructions are shown in Table 1 and Table 2. Please note that, to read data from a register, you must set R/W bit to 0 to access the register address and then set R/W to 1 to read data from the register.

Table 1 Write Data to Register in I²C Interface Mode

Chip Address		R/W		Register Address		Data to be written
001000	AD0	0	ACK	RAM	ACK	DATA

Table 2 Read Data from Register in I²C Interface Mode

Chip Address		R/W		Register Address
001000	AD0	0	ACK	RAM
Chip Address		R/W		Data to be read
001000	AD0	1	ACK	Data

6. DIGITAL AUDIO INTERFACE

The device provides many formats of serial audio data interface to the output from the ADC through LRCK, BCLK (SCLK) and ADCDAT pins. These formats are I²S, left justified and DSP/PCM mode. ADC data is out at ADCDAT on the falling edge of SCLK. The relationships of SDATA (ADCDAT), SCLK and LRCK with these formats are shown through Figure 2 to Figure 6.

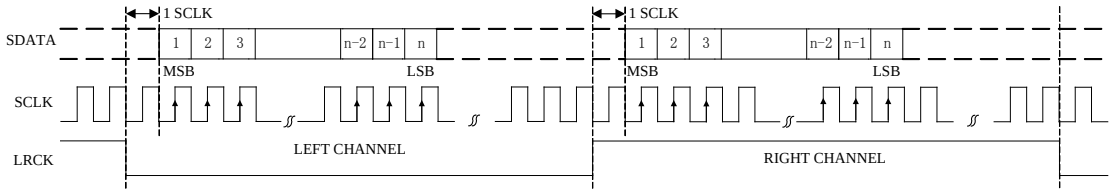


Figure 2 I²S Serial Audio Data Format Up To 24-bit

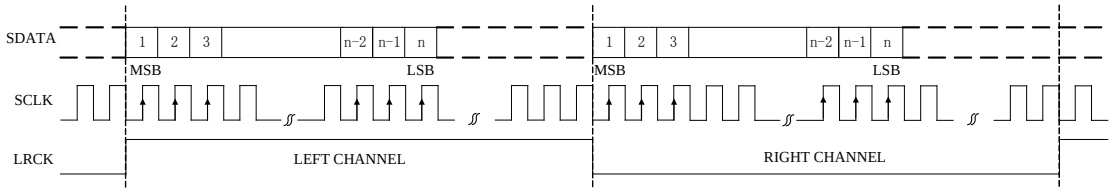


Figure 3 Left Justified Serial Audio Data Format Up To 24-bit

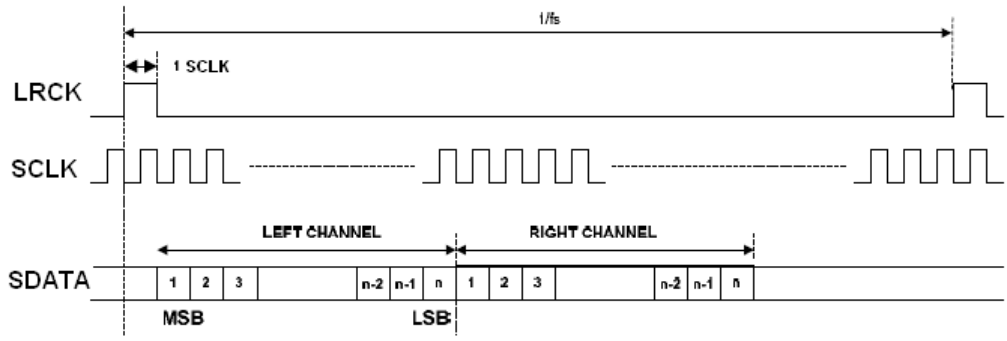


Figure 5 DSP/PCM Mode A

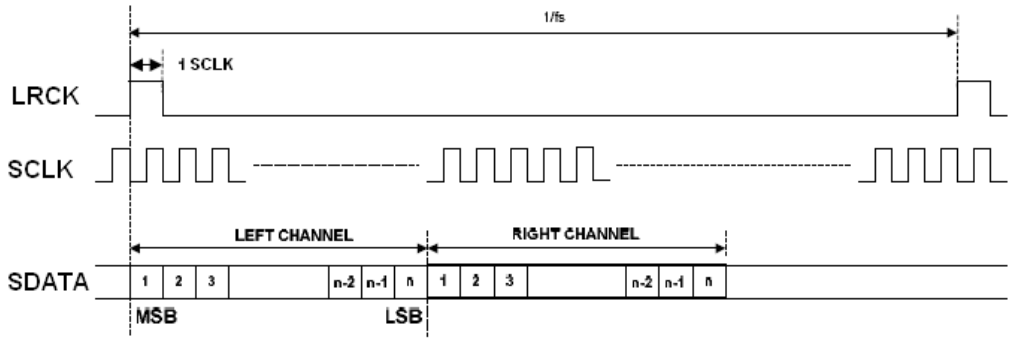


Figure 6 DSP/PCM Mode B

7. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MIN	MAX
Analog Supply Voltage Level	-0.3V	+5.0V
Digital Supply Voltage Level	-0.3V	+5.0V
Input Voltage Range	DGND-0.3V	DVDD+0.3V
Operating Temperature Range	-40°C	+85°C
Storage Temperature	-65°C	+150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
Analog Supply Voltage Level	1.6	3.3	3.6	V
Digital Supply Voltage Level	1.6	1.8	3.6	V

ADC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: AVDD=3.3V, DCVDD=1.8V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz, 96 KHz or 192 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
ADC Performance				
Signal to Noise ratio (A-weigh)	90	96	98	dB
THD+N	-88	-85	-75	dB
Gain Error			±5	%
Filter Frequency Response – Single Speed				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	50			dB
Filter Frequency Response – Double Speed				
Passband	0		0.4167	Fs
Stopband	0.5833			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	50			dB
Analog Input				
Full Scale Input Level		AVDD/3.3		Vrms
Input Impedance		20		KΩ

POWER CONSUMPTION CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
DVDD=1.8V, PVDD=1.8V, AVDD=1.8V: DVDD=3.3V, PVDD=3.3V, AVDD=3.3V:		9 28		mW
Power Down Mode				
DVDD=1.8V, PVDD=1.8V, AVDD=1.8V DVDD=3.3V, PVDD=3.3V, AVDD=3.3V		0.1 0.1		uA uA

SERIAL AUDIO PORT SWITCHING SPECIFICATIONS

PARAMETER	Symbol	MIN	MAX	UNIT
MCLK frequency			51.2	MHz
MCLK duty cycle		40	60	%
LRCK frequency			200	KHz
LRCK duty cycle		40	60	%
SCLK frequency			26	MHz
SCLK pulse width low	TSCLKL	15		ns
SCLK Pulse width high	TSCLKH	15		ns
SCLK falling to LRCK edge	TSLR	–10	10	ns
SCLK falling to SDOUT valid	TSDO	0		ns
SDIN valid to SCLK rising setup time	TSDIS	10		ns
SCLK rising to SDIN hold time	TSDIH	10		ns

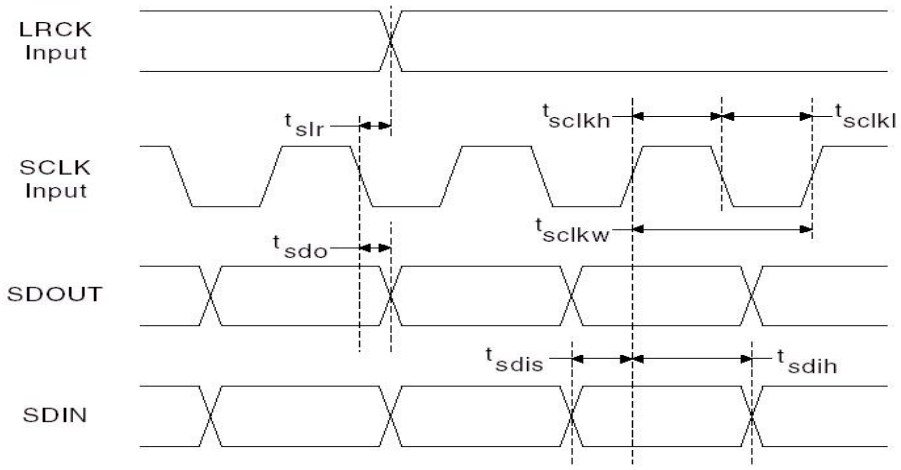


Figure 8 Serial Audio Port Timing

I²C SWITCHING SPECIFICATIONS

PARAMETER	Symbol	MIN	MAX	UNIT
SCL Clock Frequency	FSCL		400	KHz
Bus Free Time Between Transmissions	TTWID	1.3		us
Start Condition Hold Time	TTWSTH	0.6		us
Clock Low time	TTWCL	1.3		us
Clock High Time	TTWCH	0.4		us
Setup Time for Repeated Start Condition	TTWSTS	0.6		us
SDA Hold Time from SCL Falling	TTWDH		900	ns
SDA Setup time to SCL Rising	TTWDS	100		ns
Rise Time of SCL	TTWR		300	ns
Fall Time SCL	TTWF		300	ns

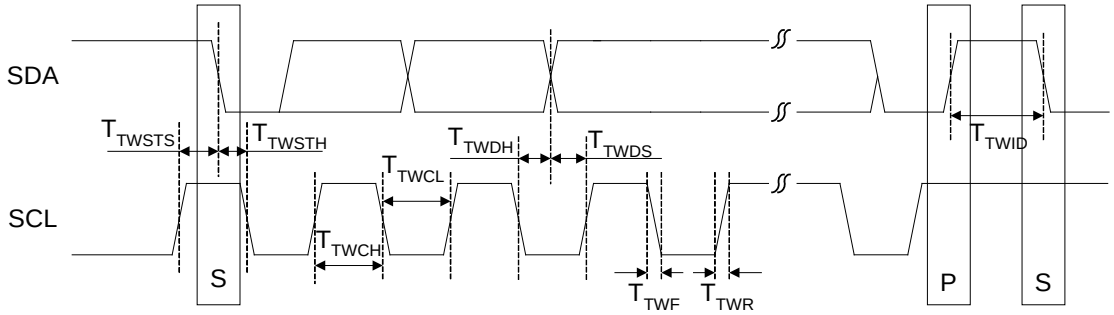


Figure 10 I²C Timing

8. CONFIGURATION REGISTER DEFINITION

REGISTER 0X0 – RESET, DEFAULT 0000 0000

Bit Name	Bit	Description
CSM_ON	7	Chip current state machine control 0 – csm power down(default) 1 – csm power on
SEQ_DIS	6	Power up/down sequence control 0 – power up sequence enable(default) 1 – power up sequence disabled
RST_DIG	5	Reset digital blocks except “cp_top” 0 – normal(default) 1 – reset digital blocks
RST_REG	4	Reset registers to default except RST_REG, write ‘0’ to release registers reset. 0 – normal (default) 1 – reset user registers to default.
RST_CLKMGR	3	reset clock manager 0 – normal (default) 1 – reset clkmgr, no clock will be generated
RST_MASTER	2	reset master block 0 – normal (default) 1 – reset master
RST_ADCDIG	1	reset ADC (include adc_dig_route and adc dsm) 0 – normal (default) 1 – reset ADC
SDP_MUTE	0	mute SDP data out 0 – normal (default) 1 – mute SDP data out

REGISTER 0X1 – CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
MSC	7	Master/Slave select 0 – slave (default) 1 – Master
GPIO_CON	6:5	GPIO control 0 – DMIC output DMIC_SCL (default) 1 – DMIC output tri-state 2 – DMIC output ‘0’ 3 – DMIC output ‘1’
MCLK_DIV2	4	MCLK be divided by 2 or not 0: normal(default) 1: divide by 2
MCLK_ON	3	MCLK in control 0: MCLK off(default) 1: MCLK on
BCLK_ON	2	BCLK in control 0: BCLK off(default) 1: BCLK on
CLK_ADC_ON	1	ADC clock divider control 0: ADC clock off(default) 1: ADC clock on

ANACLK_ADC_ON	0	ADC analog clock control 0: ADC anaclk off (default) 1: ADC anaclk on

REGISTER 0X2 – CLOCK MANAGER, DEFAULT 0000 0001

Bit Name	Bit	Description
ADCDELSEL	5	adc digclk select 0: 5ns delay(default) 1: 10ns delay
CLK_ADC_DOUBLE	4	clk_adc divide by 2 control 0 – normal(default) 1 – clk_adc divide by 2
CLK_ADC_DIV	3:0	adc_mclk clock divider f(adc_mclk)=f(MCLK) / CLK_ADC_DIV when CLK_ADC_DOUBLE=0, f(adc_mclk)= 2 * f(MCLK) / CLK_ADC_DIV when CLK_ADC_DOUBLE=1

REGISTER 0X3 – CLOCK MANAGER, DEFAULT 0010 0000

Bit Name	Bit	Description
ADC_OSR	5:0	ADC delta sigma over sample rate SS mode: adc_osr=f(adc_mclk) / fs / 8 DS mode: adc_osr=f(adc_mclk) / fs / 4 f(adc_mclk) refer to CLK_ADC_DIV and CLK_ADC_DOUBLE

REGISTER 0X4 – CLOCK MANAGER, DEFAULT 0000 0001

Bit Name	Bit	Description
ADCLRCK_DIV[11:8]	3:0	Internal adclrck divider bit 11 to bit 8

REGISTER 0X5 – CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
ADCLRCK_DIV[7:0]	7:0	Internal adclrck divider bit 7 to bit 0 LRCK=MCLK / ADCLRCK_DIG at master mode.

REGISTER 0X6 – CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
BCLK_INV	5	0 – normal (default) 1 – BCLK inverted
BCLKDIV	4:0	master mode BCLK generated 0 – no BCLK output(default) 1~18 – BCLK = MCLK/BCLKDIV 19 – BCLK = MCLK/20 20 – BCLK = MCLK/22 21 – BCLK = MCLK/24 22 – BCLK = MCLK/25 23 – BCLK = MCLK/30 24 – BCLK = MCLK/32 25 – BCLK = MCLK/33 26 – BCLK = MCLK/34 27 – BCLK = MCLK/36 28 – BCLK = MCLK/44 29 – BCLK = MCLK/48

		30 – BCLK = MCLK/66 31 – BCLK = MCLK/72

REGISTER 0X7 – SERIAL DATA PORT, DEFAULT 0000 0000

Bit Name	Bit	Description
TRI	6	Tri-state output 0 – normal 1 – ADCDAT, LRCK, BCLK tri-state output
ADCLRP	5	I2S, left justified: 0 – left and right normal polarity 1 – left and right inverted polarity DSP/PCM mode: 0 – MSB is available on 2nd BCLK rising edge after ALRCK rising edge 1 – MSB is available on 1st BCLK rising edge after ALRCK rising edge
ADCWL	4:2	000 – 24-bit serial audio data word length(default) 001 – 20-bit serial audio data word length 010 – 18-bit serial audio data word length 011 – 16-bit serial audio data word length 100 – 32-bit serial audio data word length
ADCFORMAT	1:0	00 – I2S serial audio data format(default) 01 – left justify serial audio data format 10 – reserve 11 – DSP/PCM mode serial audio data format

REGISTER 0X8 – SYSTEM CONTROL, DEFAULT 0111 1110

Bit Name	Bit	Description
PDN_ANA	7	0 – normal (default) 1 – analog power down
PDN_ADCBIASGEN	6	0 – normal 1 – adcbiasgen power down (default)
PDN_ADCVERFGEN	5	0 – normal 1 – adcvrefgen power down (default)
PDN_IBIASGEN	4	0 – normal 1 – ibiasgen power down (default)
PDN_MOD	3	0 – ADC power up 1 – ADC power down (default)
PDN_AIN	2	0 – normal 1 – analog input power down (default)
PDN_MIC	1	0 – normal 1 – micBias power down (default)
SYNCMODE	0	0 – normal (default) 1 – synchronize mode

REGISTER 0X9 – SYSTEM CONTROL, DEFAULT 0000 0000

Bit Name	Bit	Description
LPPGA	5	0 – normal power mode (default) 1 – low power mode
LPMCDF	4	0 – normal power mode (default) 1 – low power mode
LPVCMMOD	3	0 – normal power mode (default) 1 – low power mode

LPADCVRP	2	0 – normal power mode (default) 1 – low power mode
LPFLASH	1	0 – normal power mode (default) 1 – low power mode
LPINT1	0	0 – normal power mode (default) 1 – low power mode

REGISTER 0XA – SYSTEM CONTROL, DEFAULT 0000 0010

Bit Name	Bit	Description
VMIDLOW	7:6	select lower vmid option (write only) 00 – vdda/2 (default) 01 – low1, vdda/2-xxmv 10 – low2, vdda/2-xxmv 01 – low3, vdda/2-xxmv
VMIDSEL	5:4	select vmidSel option (write only) 00 – Vmid disabled 01 – 50 kΩ divider enabled 10 – 500 kΩ divider enabled(default) 11 – 5 kΩ divider enabled
VMIDLOW	3:2	observe lower vmid option (read only) 00 – vdda/2 (default) 01 – low1, vdda/2-xxmv 10 – low2, vdda/2-xxmv 01 – low3, vdda/2-xxmv
VMIDSEL	1:0	observe vmidSel option (read only) 00 – Vmid disabled 01 – 50 kΩ divider enabled 10 – 500 kΩ divider enabled(default) 11 – 5 kΩ divider enabled

REGISTER 0XB – SYSTEM CONTROL, DEFAULT 0000 0001

Bit Name	Bit	Description
IBIASGEN_MCDFSW	4	select ibiasgen_mcdf current 0 – normal(default) 1 – change bias current
IBIASGEN_PGASW	3	select ibiasgen current 0 – (default) 1 – change bias current
IBIASGEN_SW	2	select ibiasgen current 0 –normal(default) 1 – change bias current
VX2OFF	1	select vdoubler 0 – enable (default) 1 – disable
VX1SEL	0	select vdoubler voltage reference 0 – ref1 1 – ref2(default)

REGISTER 0XC – SYSTEM CONTROL, DEFAULT 1111 1100

Bit Name	Bit	Description

VSEL	7:0	11111100 – normal (default)

REGISTER 0XD – SYSTEM CONTROL, DEFAULT 0100 0000

Bit Name	Bit	Description
CHIPINI_CON	7:0	ChipIni state period control period=CHIPINI_CON*16/LRCK max=85ms

REGISTER 0XE – SYSTEM CONTROL, DEFAULT 0100 0000

Bit Name	Bit	Description
POWERUP_CON	7:0	PowerUp state period control period=POWERUP_CON*16/LRCK max=85ms

REGISTER 0XF – ADC CONTROL, DEFAULT 0001 0000

Bit Name	Bit	Description
LINSEL	5	PGA input select 0 – Lin1-Rin1 (default) 1 – Lin2-Rin2
DF2SE_18DB	4	DF2SE plus 18dB control 0 – 0dB 1 – 18dB (default)
PGAGAIN	3:0	Left PGA gain 1111 – -3.5dB 0000 – 0dB (default) 0001 – 3.5dB 0010 – 6dB 0011 – 9dB 0100 – 12dB 0101 – 15dB 0110 – 18dB 0111 – 21dB others – 0dB

REGISTER 0X10 – ADC CONTROL, DEFAULT 0001 1000

Bit Name	Bit	Description
ADCFSMODE	6	adc fs mode 0 – single speed 1 – double speed
ADCMUTE	5	ADC mute 0 – normal 1 – mute ADC volume to -96dB
ADCSOFTRAMP	4	adc soft ramp 0 – adc soft ramp disable 1 – adc soft ramp enable
ADCHPF	3	0 – disable ADC left channel high pass filter 1 – enable ADC left channel high pass filter (default)
ADCINV	2	0 – normal (default) 1 – left channel polarity inverted
DMIC_SRC	1:0	digital mic control

		0x – dmic disable 10 – DMIC high 11 – DMIC low

REGISTER 0X11 – ADC CONTROL, DEFAULT 1100 0000

Bit Name	Bit	Description
adcVolumeL	7:0	00000000 — 0dB 00000001 — -0.5dB 00000010 — -1dB … 11000000 — -96dB(default)

REGISTER 0X12 – ADC CONTROL, DEFAULT 0001 1100

Bit Name	Bit	Description
ALCSEL	7:6	00 — alc off other — alc on
ALCMODE	5	Determines the ALC mode of operation: 0 – ALC mode (Normal Operation) 1 – Limiter mode.
MAXGAIN[4:0]	4:0	ALC MAXGAIN[1:0] for PGA max gain 00000 – -6.5dB 00001 – -5 dB 00010 – -3.5dB 00011 – -2dB 00100 – -0.5dB 00101 – +1dB 00100 – +2.5dB 00111 – +4dB 01000 – +5.5dB 01001 – +7dB 01010 – +8.5dB 01011 – +10dB 01100 – +11.5dB 01101 – +13dB 01110 – +14.5dB 01111– +16dB 10000 – +17.5dB 10001 – +19dB 10010 – +20.5dB 10011 – +22dB 10100 – +23.5dB 10101 – +25dB 10110 – +26.5dB 10111 – +28dB 11000 – +29.5dB 11001 – +31dB 11010 – +32.5dB 11011 – +34dB others – +35.5dB

REGISTER 0X13 – ADC CONTROL, DEFAULT 0000 0000

Bit Name	Bit	Description
MINGAIN[4:0]	4:0	ALC MINGAIN[1:0] for PGA min gain 00000 – -12dB 00001 – -10.5 dB 00010 – -9dB 00011 – -7.5dB 00100 – -6dB 00101 – -4.5dB 00100 – -3dB 00111 – -1.5dB 01000 – 0dB 01001 – +1.5dB 01010 – +3dB 01011 – +4.5dB 01100 – +6dB 01101 – +7.5dB 01110 – +9dB 01111– +10.5dB 10000 – +12dB 10001 – +13.5dB 10010 – +15dB 10011 – +16.5dB 10100 – +18dB 10101 – +19.5dB 10110 – +21dB 10111 – +22.5dB 11000 – +24dB 11001 – +25.5dB 11010 – +27dB 11011 – +28.5dB others – +30dB

REGISTER 0X14 – ADC CONTROL, DEFAULT 1011 0000

Bit Name	Bit	Description
ALCLVL	7:4	ALC target 0000 – -16.5 dB 0001 – -15 dB 0010 – -13.5 dB …… 0111 – -6 dB 1000 – -4.5 dB 1001 – -3 dB 1010-1111 – -1.5 dB
ALCHLD	3:0	ALC hold time before gain is increased 0000 – 0ms 0001 – 2.67ms 0010 – 5.33ms …… (time doubles with every step) 1001 – 0.68s 1010 or higher – 1.36s

REGISTER 0X15 – ADC CONTROL, DEFAULT 0011 0010

Bit Name	Bit	Description
ALCDCY	7:4	ALC decay (gain ramp up) time at ALC mode/limiter mode: 0000 – 410 us/90.8 us 0001 – 820 us/182us 0010 – 1.64 ms/363us …… (time doubles with every step) 1001 – 210 ms/46.5 ms 1010 or higher – 420 ms/93 ms
ALCATK	3:0	ALC attack (gain ramp down) time at ALC mode/limiter mode: 0000 – 104 us/22.7 us 0001 – 208 us/45.4 us 0010 – 416 us/90.8 us …… (time doubles with very step) 1001 – 53.2 ms/11.6 ms 1010 or higher – 106 ms/23.2 ms

REGISTER 0X16 – ADC CONTROL, DEFAULT 0000 0011

Bit Name	Bit	Description
WIN_SIZE	4:0	Windows size for peak detector， set the window size to N*16 samples 00110 – 96 samples (default) 00111 – 102 samples ….. 11111 – 496 samples

REGISTER 0X17 – ADC CONTROL, DEFAULT 0000 0000

Bit Name	Bit	Description
ALC_NGG	6	noise gate type 0 – original gain(default) 1 – mute
ALC_NGAT	5	noise gate enable 0 – disable(default) 1 – enable
ALC_NGTH	4:0	Noise gate threshold 00000 – -76.5 dBFS 00001 – -75 dBFS …… 11110 – -31.5 dBFS 11111 – -30 dBFS

REGISTER 0X18 – ADC CONTROL, DEFAULT 0000 1101

Bit Name	Bit	Description
HPF_COEFF_S	4:0	HPF slow settling coeff

REGISTER 0X19 – ADC CONTROL, DEFAULT 0000 0110

Bit Name	Bit	Description
HPF_COEFF_F	4:0	HPF fast settling coeff

REGISTER 0X1A – ADC CONTROL , DEFAULT 0001 1111

Bit Name	Bit	Description
shelving1_a[29:24]	5:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 0X1B – ADC CONTROL, DEFAULT 1111 0111

Bit Name	Bit	Description
shelving1_a[23:16]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 0X1C – ADC CONTROL, DEFAULT 1111 1101

Bit Name	Bit	Description
shelving1_a[15:8]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 0X1D – ADC CONTROL, DEFAULT 1111 1111

Bit Name	Bit	Description
shelving1_a[7:0]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 0X1E – ADC CONTROL, DEFAULT 0001 1111

Bit Name	Bit	Description
shelving1_b[29:24]	5:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 0X1F – ADC CONTROL, DEFAULT 1111 0111

Bit Name	Bit	Description
shelving1_b[23:16]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 0X20 – ADC CONTROL, DEFAULT 1111 1101

Bit Name	Bit	Description
shelving1_b[15:8]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 0X21 – ADC CONTROL, DEFAULT 1111 1111

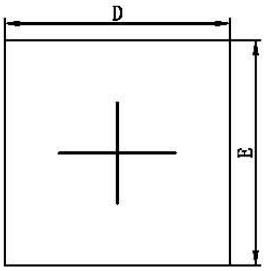
Bit Name	Bit	Description
shelving1_b[7:0]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 0X22 – FLAG, DEFAULT 0000 0000

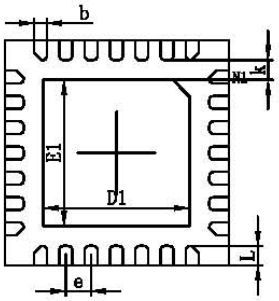
Bit Name	Bit	Description
FLAG_MASTER_ERR	2	master error flag(read only)
FLAG_CSM	1:0	CSM flag (read only) 00: PowDown 01: ChipIni 11: PowerUp 10: Normal

9. PACKAGE

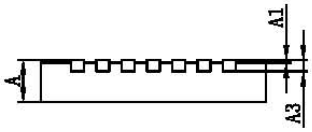
QFNWB4×4-28L-A(P0.45T0.75/0.85)PACKAGE OUTLINE DIMENSIONS



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.924	4.076	0.154	0.160
E	3.924	4.076	0.154	0.160
E1	2.500	2.700	0.098	0.106
D1	2.500	2.700	0.098	0.106
k	0.200MIN		0.008MIN	
b	0.180	0.280	0.007	0.011
e	0.450TYP.		0.018TYP.	
L	0.274	0.426	0.011	0.017

10.CORPORATE INFORMATION

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