ES7242

High Performance Stereo Audio ADC

FEATURES

- High performance multi-bit delta-sigma audio ADC
- 100 dB signal to noise ratio
- -85 dB THD+N
- 3 Vpp analog input
- 24-bit, 8 to 200 kHz sampling frequency
- I^2S/PCM master or slave serial data port
- Support TDM
- 256/384Fs, USB 12/24 MHz and other non standard audio system clocks
- Low power standby mode

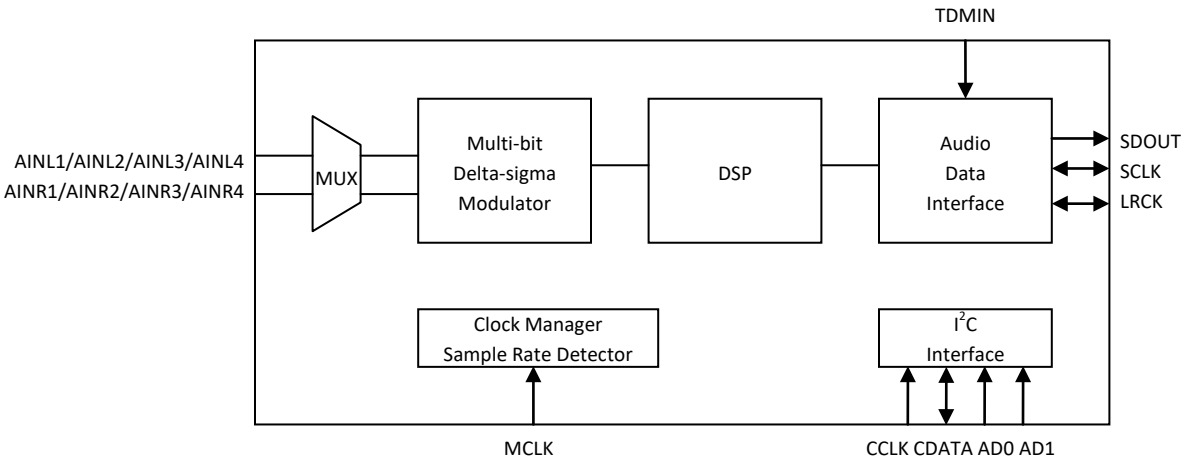
APPLICATIONS

- Soundbar
- Audio Interface
- Digital TV
- A/V Receiver
- DVR
- NVR

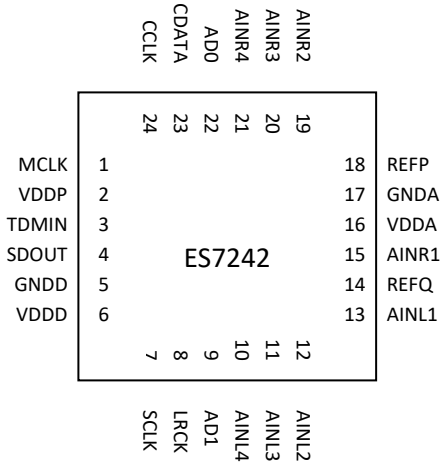
ORDERING INFORMATION

ES7242 -40°C ~ +85°C
QFN-24

BLOCK DIAGRAM

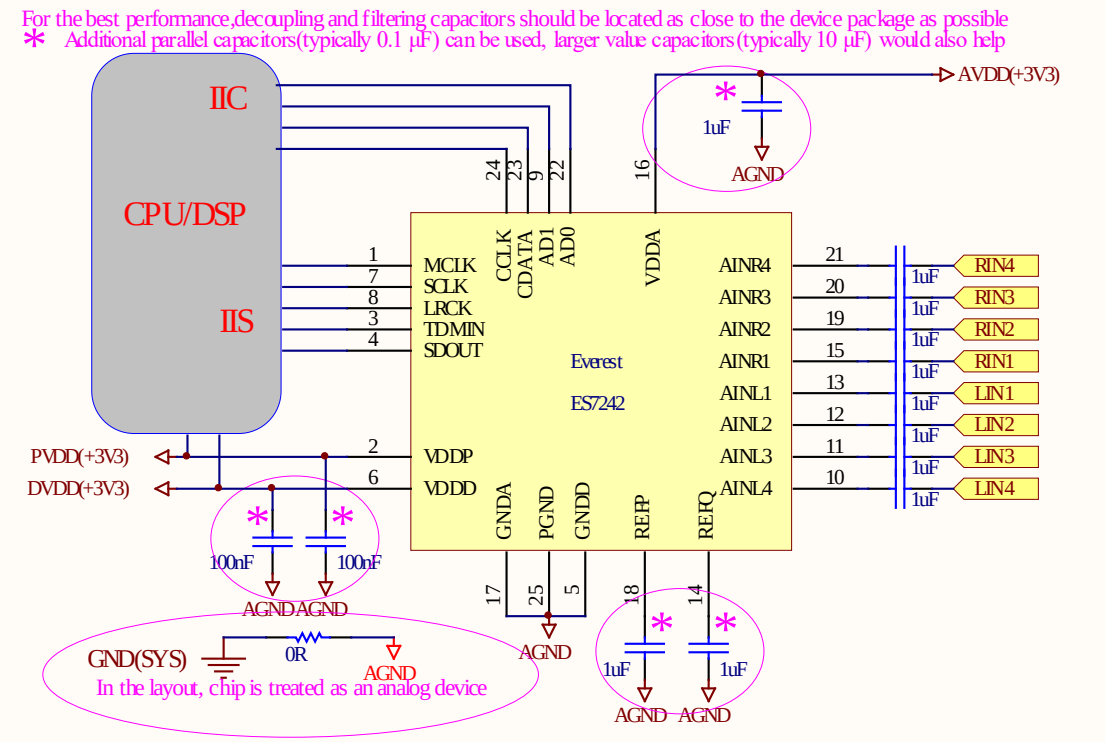


1. PIN OUT AND DESCRIPTION



Pin Name	Pin number	Input or Output	Pin Description
CCLK, CDATA	24, 23	I/O	I^2C clock and data
AD0, AD1	22, 9	I	I^2C addresses
MCLK	1	I	Master clock
SCLK	7	I/O	Serial data bit clock
LRCK	8	I/O	Serial data left and right channel frame clock
TDMIN	3	I	TDM data in
SDOUT	4	O	Serial data output
AINL1, AINR1 AINL2, AINR2 AINL3, AINR3 AINL4, AINR4	13, 15 12, 19 11, 20 10, 21	I	Analog left and right inputs
VDDP	2	I	Power supply for the digital input and output
VDDD/GNDD	6, 5	I	Digital power supply
VDDA/GNDA	16, 17	I	Analog power supply
REFP	18	O	Filtering capacitor connection
REFQ	14	O	Filtering capacitor connection

2. TYPICAL APPLICATION CIRCUIT



3. CLOCK MODES AND SAMPLING FREQUENCIES

The device supports standard audio clocks (256Fs, 384Fs, 512Fs, etc), USB clocks (12/24 MHz), and some common non standard audio clocks (25 MHz, 26 MHz, etc).

According to the serial audio data sampling frequency (Fs), the device can work in two speed modes: single speed mode or double speed mode. In single speed mode, Fs normally ranges from 8 kHz to 48 kHz, and in double speed mode, Fs normally range from 64 kHz to 96 kHz.

The device can work either in master clock mode or slave clock mode. In slave mode, LRCK and SCLK are supplied externally, and LRCK and SCLK must be synchronously derived from the system clock with specific rates. In master mode, LRCK and SCLK are derived internally from device master clock.

4. MICRO-CONTROLLER CONFIGURATION INTERFACE

The device supports standard I^2C micro-controller configuration interface. External micro-controller can completely configure the device through writing to internal configuration registers.

I^2C interface is a bi-directional serial bus that uses a serial data line (CDATA) and a serial clock line (CCLK) for data transfer. The timing diagram for data transfer of this interface is given in Figure 1a and Figure 1b. Data are transmitted synchronously to CCLK clock on the CDATA line on a byte-by-byte basis. Each bit in a byte is sampled during CCLK high with MSB bit being transmitted firstly. Each transferred byte is followed by an acknowledge bit from receiver to pull the CDATA low. The transfer rate of this interface can be up to 400 kbps.

A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at CDATA while CCLK is high. The first byte transferred is the slave address. It is a seven-bit chip address followed by a RW bit. The chip address must be 0010 0x, where x equals ~AD1 ~AD0. The RW bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the RW bit. The master can terminate the communication by generating a “stop” signal, which is defined as a low-to-high transition at CDATA while CCLK is high.

In I^2C interface mode, the registers can be written and read. The formats of “write” and “read” instructions are shown in Table 1 and Table 2. Please note that, to read data from a register, you must set R/W bit to 0 to access the register address and then set R/W to 1 to read data from the register.

Table 1 Write Data to Register in I^2C Interface Mode

	Chip Address	R/W		Register Address		Data to be written		
start	0010 0 ~AD1 ~AD0	0	ACK	RAM	ACK	DATA	ACK	Stop

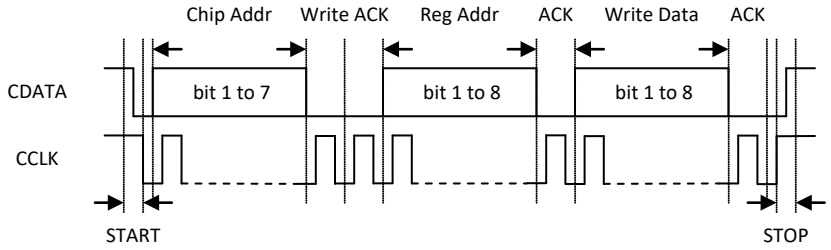


Figure 1a I²C Write Timing

Table 2 Read Data from Register in I²C Interface Mode

	Chip Address	R/W		Register Address		
Start	0010 0 ~AD1 ~AD0	0	ACK	RAM	ACK	
	Chip Address	R/W		Data to be read		
Start	0010 0 ~AD1 ~AD0	1	ACK	Data	NACK	Stop

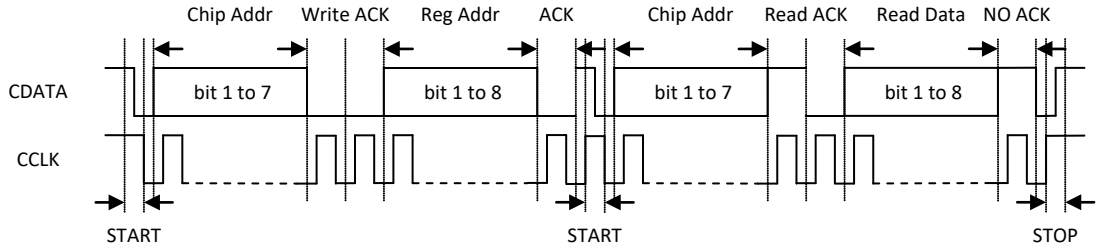


Figure 1b I²C Read Timing

5. DIGITAL AUDIO INTERFACE

The device provides many formats of serial audio data interface to the output from the ADC through LRCK, SCLK and SDOUT pins. These formats are I²S, left justified and DSP/PCM mode. ADC data is out at SDOUT on the falling edge of SCLK. The relationships of SDOUT (SDATA), SCLK and LRCK with these formats are shown through Figure 2 to Figure 5.

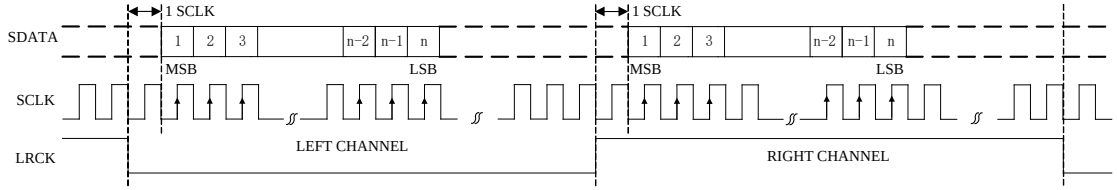


Figure 2 I²S Serial Audio Data Format Up To 24-bit

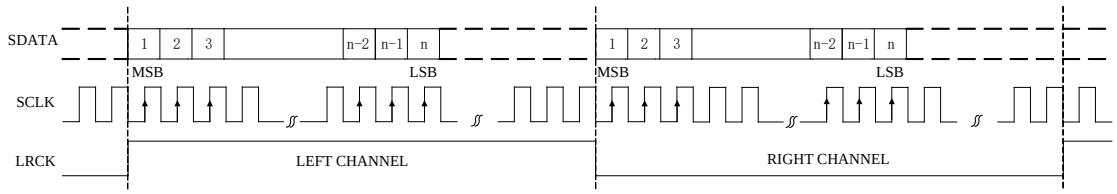


Figure 3 Left Justified Serial Audio Data Format Up To 24-bit

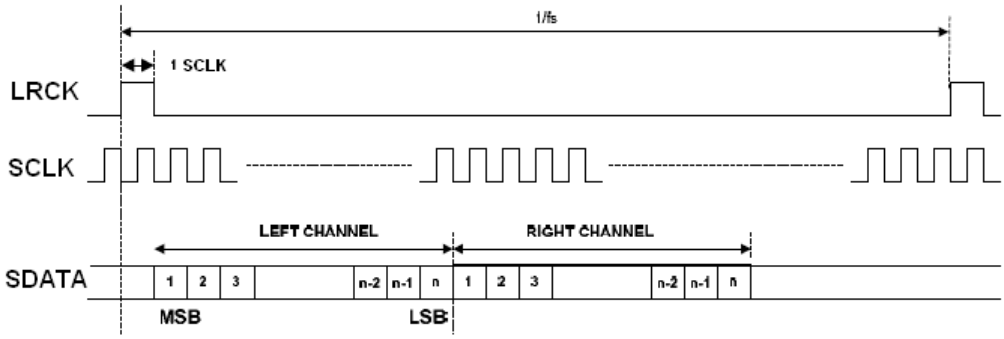


Figure 4 DSP/PCM Mode A

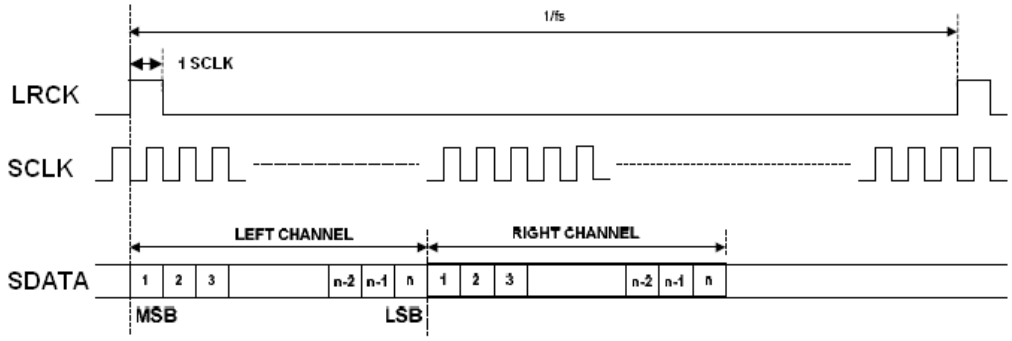


Figure 5 DSP/PCM Mode B

6. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MIN	MAX
Analog Supply Voltage Level	-0.3V	+3.6V
Digital Supply Voltage Level	-0.3V	+3.6V
Analog Input Voltage Range	GNDA-0.3V	VDDA+0.3V
Digital Input Voltage Range	GNDD-0.3V	VDDP+0.3V
Operating Temperature Range	-40°C	+85°C
Storage Temperature	-65°C	+150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
VDDA	3.0	3.3	3.6	V
VDDD	3.0	3.3	3.6	V
VDDP	1.6	3.3	3.6	V

ADC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: VDDA=3.3V, VDDD=3.3V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz, 96 KHz or 192 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
ADC Performance				
Signal to Noise ratio (A-weigh)	95	100	104	dB
THD+N	-88	-85	-75	dB
Channel Separation (1KHz)	95	100	105	dB
Interchannel Gain Mismatch		0.1		dB
Gain Error			±5	%
Filter Frequency Response – Single Speed				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	70			dB
Filter Frequency Response – Double Speed				
Passband	0		0.4167	Fs
Stopband	0.7917			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	70			dB
Filter Frequency Response – Quad Speed				
Passband	0		0.2083	Fs
Stopband	0.8958			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	70			dB
Analog Input				
Full Scale Input Level		3		Vpp
Input Impedance		20		KΩ

Note: there are phase inversions between analog input and digital output for both left and right channels. For customers who care about the phase inversions, reverse of phase inversions should be performed in post processing DSP or host, or in wiring of speaker terminals.

DC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
VDDD=3.3V, VDDP=3.3V, VDDA=3.3V		14		mA
Power Down Mode				

VDDD=3.3V, VDDP=3.3V, VDDA=3.3V		19		uA
Digital Voltage Level				
Input High-level Voltage	0.7*VDDP			V
Input Low-level Voltage			0.5	V
Output High-level Voltage		VDDP		V
Output Low-level Voltage		0		V

SERIAL AUDIO PORT SWITCHING SPECIFICATIONS

PARAMETER	Symbol	MIN	MAX	UNIT
MCLK frequency			49.2	MHz
MCLK duty cycle		40	60	%
LRCK frequency			200	KHz
LRCK duty cycle (Note 1)		40	60	%
SCLK frequency			26	MHz
SCLK pulse width low	T_{SLKL}	16		ns
SCLK Pulse width high	T_{SCLKH}	16		ns
SCLK falling to LRCK edge (master mode only)	T_{SLR}		10	ns
LRCK edge to SCLK rising (slave mode only)	T_{LSR}	10		ns
SCLK falling to SDOUT valid VDDD=3.3V	T_{SDO}		16	ns
LRCK edge to SDOUT valid (Note 2) VDDD=3.3V	T_{LDO}		11	ns

Note 1: one SCLK period of high time in DSP/PCM modes.

Note 2: only apply to MSB of Left Justified or DSP/PCM mode B.

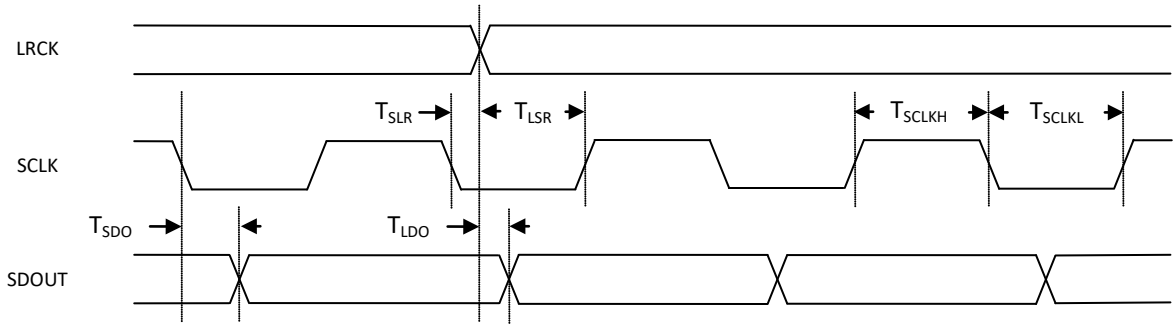


Figure 6 Serial Audio Port Timing

I^2C SWITCHING SPECIFICATIONS (SLOW SPEED MODE/HIGH SPEED MODE)

PARAMETER	Symbol	MIN	MAX	UNIT
CCLK Clock Frequency	F_{CCLK}		100/400	KHz
Bus Free Time Between Transmissions	T_{TWID}	4.7/1.3		us
Start Condition Hold Time	T_{TWSTH}	4.0/0.6		us
Clock Low time	T_{TWCL}	4.7/1.3		us
Clock High Time	T_{TWCH}	4.0/0.6		us
Setup Time for Repeated Start Condition	T_{TWSTS}	4.7/0.6		us
CDATA Hold Time from CCLK Falling	T_{TWDH}		3.45/0.9	us
CDATA Setup time to CCLK Rising	T_{TWDS}	0.25/0.1		us
Rise Time of CCLK	T_{TWR}		1.0/0.3	us

Fall Time CCLK	T_{TWF}		1.0/0.3	us

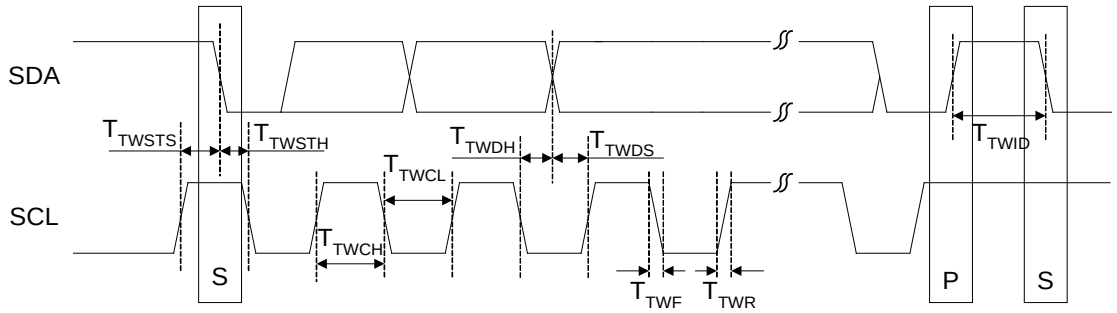
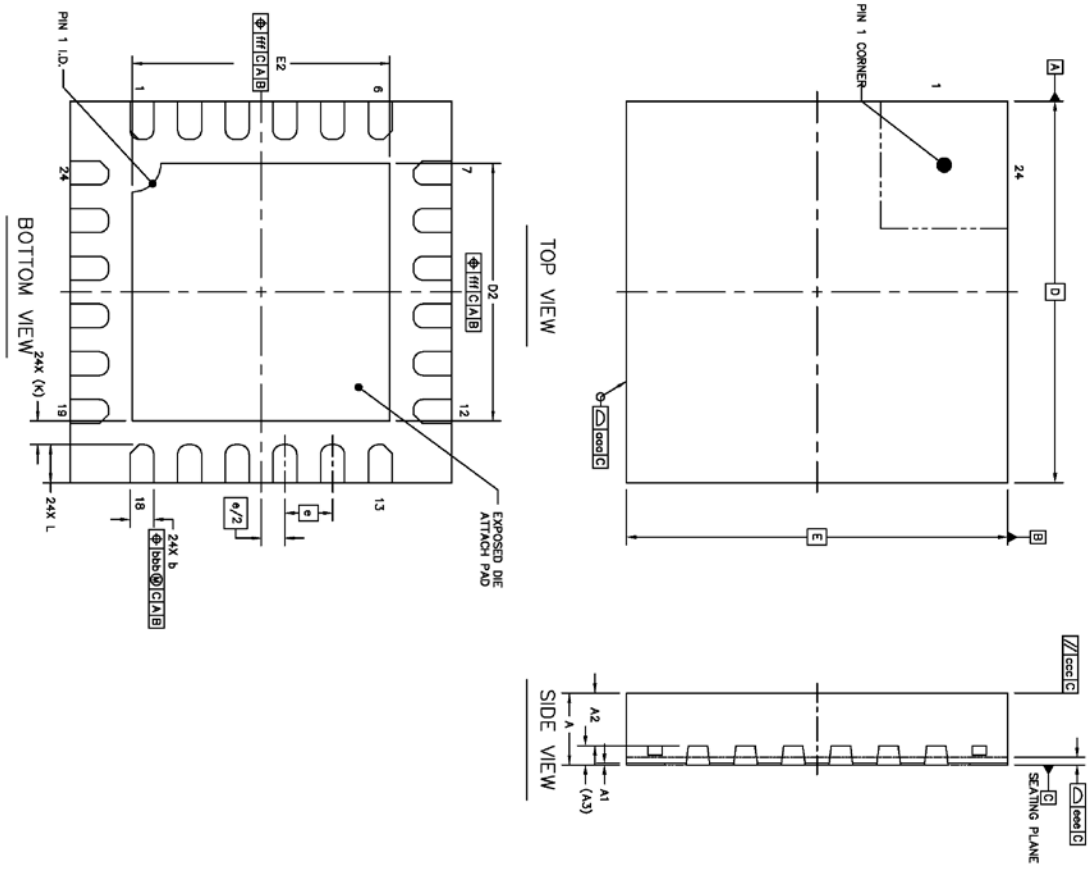


Figure 7 I^2C Timing

7. PACKAGE



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	2.6	2.7	2.8
	Y	E2	2.6	2.7	2.8
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.25REF.	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

8. CORPORATE INFORMATION

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